



• Towards a Generic Foundry Model Glass, Silicon and InP

• (Generic) Circuit approach Building Blocks, Design rules, Design kits

• Opportunities

Jeppix, ePIXfab, OpSIS ...





(vertical integrated fab)

Since 1990 worldwide several B\$ invested in development of photonic integration technologies

Market share of PICs is still small for payback investments

- Almost all research was strongly application driven
- No coordination in technology development
- Therefore, almost as many technologies as applications
- No knowledge and cost sharing advantage
- For most companies entry costs too high
- Move to a few generic technologies that support a broad range of functionalities
- > Apply the methodology of CMOS to photonics

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- Up to now almost all research has been Application driven
- Therefore almost as many technologies as applications (almost everything is reinvented)
- For most of them: market too small for payback investments
- Huge fragmentation, unsustainable fragments
- (in electronic) Huge market served by a small set of integration technologies
- (in photonic) Small market served by a huge set of integration technologies

A fully optimized technology for a succesfull application

Too many degree of freedom, Too many materials, Too many technologies, Too many component types, too many packaging types **No standards**

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... that support a broad range of functionalities

Limit the number of possibilities (technologies, devices, materials, dimensions, ...)

Move to a Generic Foundry Model means

- Convergence of technologies
- Decouple design and technology (IP)
- Reduce cost (entry, development, qualification, multi-projects...)
- Use standard Building Blocks
- Set up libraries, design kits, circuit design tools
- Generic packaging

Fabless companies, new market, design houses, high quality foundries, reduced time to market, no custom design...





... that support a broad range of functionalities



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Move from *application specific* technology development to *generic* technologies that apply to a broad range of functionalities

Apply the methodology of microelectronics to photonics

| Knowledge and cost sharing | Vertical Integrated Model | Custom Foundry Model | Generic Foundry Model |
|----------------------------|---------------------------------|----------------------------|-----------------------------|
| Cleanroom fab | NO | YES | YES |
| Integration process | NO | NO | YES |
| Design Kit | NO | NO | YES |
| Component Library | NO | NO | YES |
| Packaging | NO | NO | YES |
| Qualification and testing | NO | NO | YES |



The generic foundry model (in Europe)





Eco-system for InP foundry model





JePPIX: broker InP and TriPleX

TU/e Technische Universiteit Eindhoven University of Technology

Value chain for photonic ASICs prototyping

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Multi-Project Wafer (MPW) runs



Generic foundries offer standardized and general-purpose fabrication technologies to external users. The ecosystem of fabless player can focus on new circuital solutions rather than technological issues.

Learning from integrated electronics

- Access to a cutting-edge photonic technology
- Sharing wafer: sharing fab costs
- Simple and cheap way of prototyping
- Fabless business model





Increasing complexity

Increase of complexity:

- At the ASPICs level
- At the mask/reticle level



Photonic ICs : variety of applications

> 350 ASPICs fabricated in MPW runs





All-optical regenerator for constant envelope WDM signals



WDM to TDM Trans-Multiplexer



Pulse serialiser



Brillouin strain sensor readout

Fiber sensor readout



Fiber Bragg Grating readout



Fiber Bragg Grating readout

Medical and bio-imaging



Pulse shaper for bio-imaging



Integrated tunable laser for optical coherence tomography

THz Optical to RF converter



Variety of lasers



Widely tunable ring laser



Variable repetition rate pulse laser



Filtered-feedback multi-wavelength laser

tunable laser with integrated MZI modulator

QPSK receiver



Optical switching



4x4 space and wavelength selective switch



Fast optical switch matrix

Fiber to the home



WDM receiver



WDM transmitter

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Major Generic foundries





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MICRO FOUNDRY

http://www.jeppix.eu

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GLOBALFOUNDRIES Capacity: ~7M Wafers/Yr*

| East Fishkill, New York | Malta, New York | Burlington, Vermont | Dresden, Germany | Singapore | |
|----------------------------|----------------------|------------------------|---------------------|----------------------------------|--|
| | | | | | |
| TECHNOLOGY | | | | | |
| 90nm–22nm | 28nm, ≤ 14nm | 350nm–90nm | 45nm-22nm | 180nm–40nm | |
| CAPACITY IN WAFERS/MONTH | | | | | |
| 14,000 (300mm) | Up to 60,000 (300mm) | 40,000 (200mm) | 60,000 (300mm) | 68,000 (300mm) 93,000 (200mm) | |

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The (potential) market forecast



























COMPARISON OF FULLY INTEGRATED SILICON PHOTONICS MPW PLATFORM (WITH PASSIVES AND ACTIVES) AVAILABLE IN R&D FOUNDRIES

| | IME/OpSIS | IMEC/ePIXfab | CEA-LETI/ ePIXfab |
|--------------------------------------|--|--|--|
| Passives | Si passives with 60nm, 130 nm and 220 nm etch depths | Si passives with 70nm, 130 nm and 220 nm etch depths, extra poly-Si layer | Si passives with 70nm, 130 nm and 220 nm etch depths |
| Photodetector | Ge vertical pin | Ge vertical pin | Ge lateral pin |
| Modulator | Si MZ, Si ring | Si MZ, Si ring | Si MZ |
| Heater ¹ | doped Si | doped Si | |
| Couplers | Vertical and edge | Vertical | Vertical |
| Wavelength Supported ² | 1310 and 1550 nm | 1310 and 1550 nm | 1550 nm |
| CAD Tools | Mentor Graphics/ Lumerical | Mentor Graphics/ IPKISS/Phoenix | Mentor Graphics/ Phoenix |
| Packaging | PLC Connections/ Chiral | Tyndall National Institute | Tyndall National Institute |
| Pricing ³ | \$1800 - 2200 USD/mm ² | \$1330 - 1550 EUR/mm ² | \$1400 - 2500 EUR/mm ² |





ROADMAP • FREE ARTICLE

Roadmap on silicon photonics

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http://www.jeppix.eu

IPSR ROADMAP

https://aimphotonics.academy/roadmap/ipsr-roadmap



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DWDM on CWDM - Aspic
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Logical process flow





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Analysis, design, study of large and complete optical circuits



• The key point is the 'model', which describes the behavior of the circuits' building blocks

• The **BBs** are described by models that collect all the microscopic details and to be used at macroscopic level



Electromagnetic approach (physical modeling)

Circuit approach (high abstraction level)

$$\nabla \times \mathbf{E} = -j\omega\mathbf{B}$$
$$\nabla \times \mathbf{H} = j\omega\mathbf{D} + \mathbf{J}$$
$$\mathbf{B} = \mu\mathbf{H}$$
$$\nabla \cdot \mathbf{D} = \rho$$

- flexible (no modeling required)
- needs and gives physical parameters
- large time and memory requirements
- suitable for small elements

- requires a modeling
- non information on geometry & materials
- access only to input/output port waves
- very fast, suitable for large circuits







The wave equation: $\nabla^2 \mathbf{E_t} + \nabla (\mathbf{E_t} \cdot \nabla \ln \varepsilon) + (\omega^2 \varepsilon \mu_0 - \beta^2) \mathbf{E_t} = \mathbf{0}$ BPM, FDTD, FEM, EME, MoL, MM, IE,







The model / BB / S matrix



- higher abstraction level
- model (preprocessing)
- single/multi mode
- measure/datasheets/EM results



Modelling of photonic Building Blocks





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The model of a straight waveguide





- α , β $f(\lambda, temperature, I, V, E and H field, statistics, aging ... solar wind, radioactivity !)$
- *TE / TM: birefringence, multimode, mode coupling,...*
- Input/output modal mismatch
- Parasitic interactions, backscatter
- Nonlinearities

• /

• $e^{-\alpha L - j\beta L}$





The Building Blocks





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The Composite Building Blocks













Some physical Building Blocks





















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The (SOI) Building Blocks Library





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Photonic integration







4 basic elements 3 basic elements PWD ERM SOA Waveguide **PWD** ERM Phase SO/ Amplitude Polarisation

Electronic integration





Integration of building blocks in a single chip





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All kinds of passive devices ...







switches and modulators ...







All kinds of lasers ...











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BB comes from a cooperation: Foundry + Designer + BB builder



Effective index n_{eff} is the most important parameter

Effective index n_{eff} is useless !

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Circuit = Σ Building Blocks





Tunable delay line 0÷8 bit @ 10...100 Gbit/s OOK, 10 Gbit/s















Functionality —> Topology

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Fill the gap between components and systems





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CITCUIT SIMULATOR





Product

 ASPIC is a software for the analysis and design of integrated and hybrid optical circuits without restrictions in dimensions and complexity. Its model-based approach does not need descriptions at physical level, permitting to concentrate on the circuit functionality.

 ASPIC is complementary to classical electromagnetic simulators and is many orders of magnitude faster and less memory consuming.

 ASPIC is a powerful environment that allows to analyze complete optical circuits, calculate the spectral behavior, synthesize devices, realize virtual experiments, carry out 'what if' and 'worst case' analysis, compare measurements and simulations for parameter extraction, estimate the yield, study the impact of technological tolerances and much more...

 ASPIC can be used for "educational", "proof of concept", "research" and "virtual prototyping" purposes and will be your precious, invaluable and powerful tool to develop optical devices and circuits

| Login | | |
|----------------|----------------------|--|
| Login | | |
| Password | | |
| Login | | |
| Register to de | ownload demo version | |





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Analysis of the circuit



Each element of the circuit has N ports where the complex amplitudes of input and output waves are specified.

Each element is described by a Scattering matrix

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Matrix description of the circuit







Structure of a circuit simulator (ASPIC)





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n_{eff} Etching depth Layers thickness Material homogeneity Stress & Strain Linewidth

> Wafer ME2768 Etch depth 60 min



$$K = \sin^2(\kappa L) = \sin^2(\kappa_0 e^{-g/d}L)$$



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1.92

1.90

1.88

Etch depth [um]

1.94

1.96

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Tolerance impact on filters (δn_{eff} , δk)









Tolerance on coupling coefficients and effective index







Tunable delay line







A matrix of rings...



Robust optical delay lines with topological protection M. Hafezi, NATURE PHYSICS, VOL. 7, NOVEMBER 2011



1656 Building Blocks, 3760 ports, 18 nested variables

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Libraries for ASPIC[™] simulator





1600 BBs; 100 lambda points \rightarrow 1 min

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