From singulated devices to wafer level testing: requirements & challenges

EPIC Meeting on Testing of Optoelectronics, Belfast, 16th February 2018

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ficonTEC

A year ago in Pisa …..

- The subject of testing for PICs and other photonics devices within the EPIC 'community' was first discussed in Pisa a year ago
- ficonTEC is better known for automated assembly, but we do a fair amount of testing
- My presentation is NOT a lecture on photonics testing …
- I want to share some of the results and continue the discussion on requirements and challenges
- I seek all the collaboration we can get with other partners to target and cover ALL aspects of high volume testing: mechanical positioning, mixed electrical & optical probing, instrumentation, test protocols, ..
- It is very appropriate that we meet at YELO and I thank our hosts and EPIC for gathering us here today

Our mission / what we do

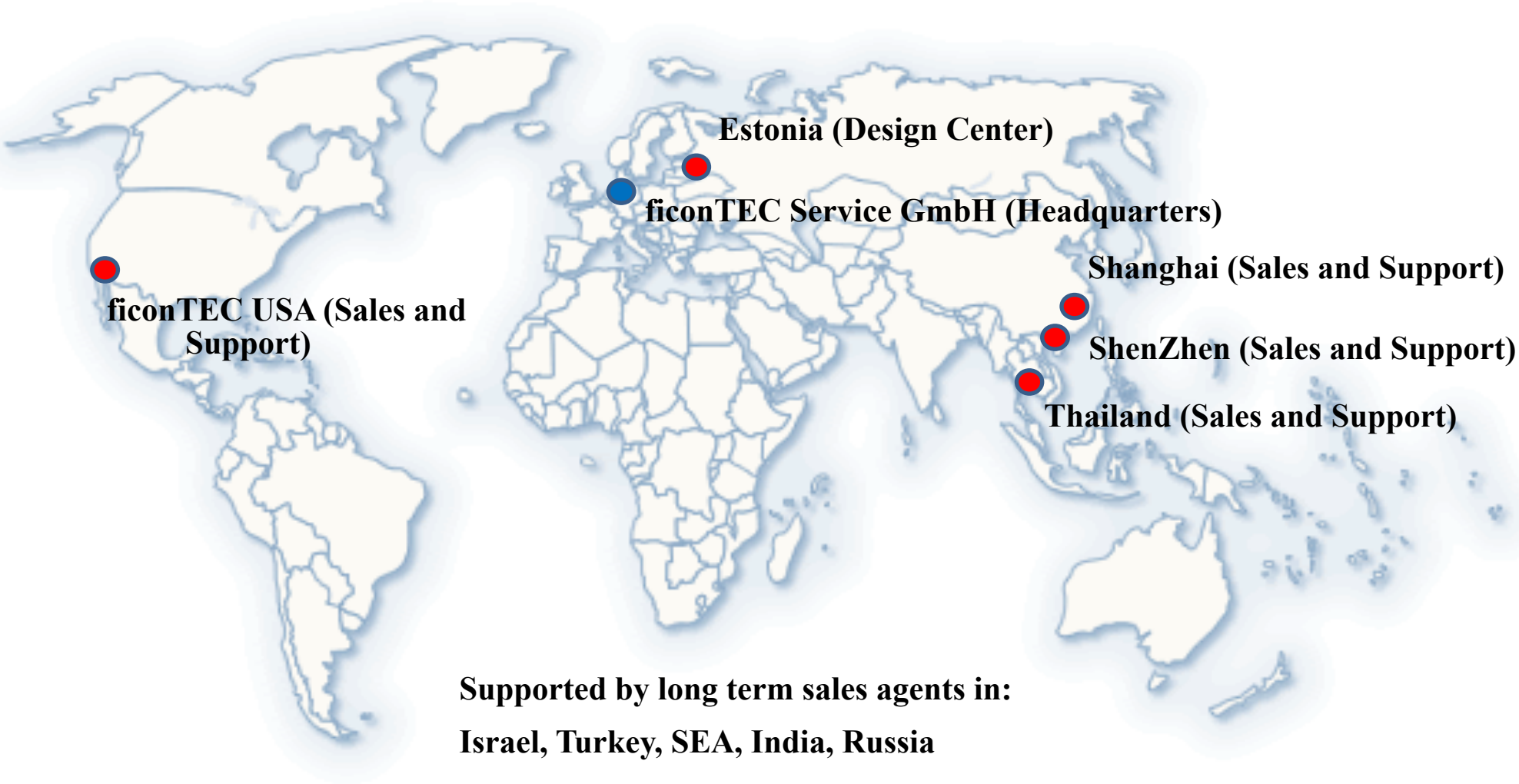
- We are a machines manufacturer for medium and high volume micro-assembly and test of PIC devices
- **Our machines are the 'embodiment' of customer process needs**
- Customized machines tailored to customers requirements based on a modular platform
- > 200 employees mainly engineers with photonics and mechatronic engineering background
- > 500 machines shipped to the biggest photonic companies world wide with support teams in China, US, Thailand and Taiwan
- **A SME company 'playing' with giants ….**

Multi-Solution | One-Source

ficonTEC assembly automation solutions

Laser Diode Stacking Testing & Characterization	Laser and PD DieBonding	Lens Attach and complex optical subassemblies	Fiber Attach Processes	Final Test/ Characterization
• Stacking-Unstacking • LD/LD Bar Handling • Facet coating • Visual inspection	• Laser Diodes/Photo Diodes • Passive/Active • Integrated Optics • Laser Soldering • Conventional heating	• Active Alignment • Lens and Array Assemlby • Epoxy bonding • Thermal cure • different dispens methods • Full/Semi automatic	• Fiber to Pump Assy • Fiber Array Attachment • Autom[illegible] fiber handling • [illegible]ng [illegible] Soldering	•Final Module Test • Handling to/from BurnIn carrier • Supply of customized test equippment based on PXI

Strong International Presence (90% Export)

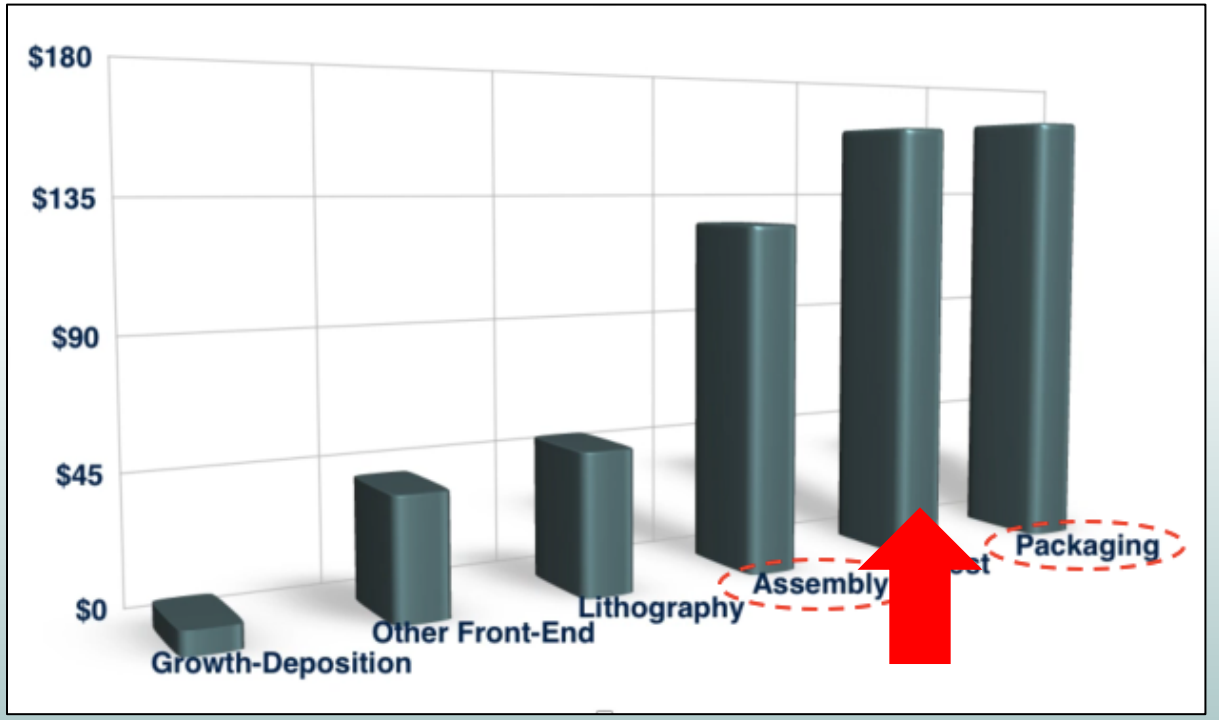


Supported by long term sales agents in:

Israel, Turkey, SEA, India, Russia

Assembly / **testing** / packaging costs

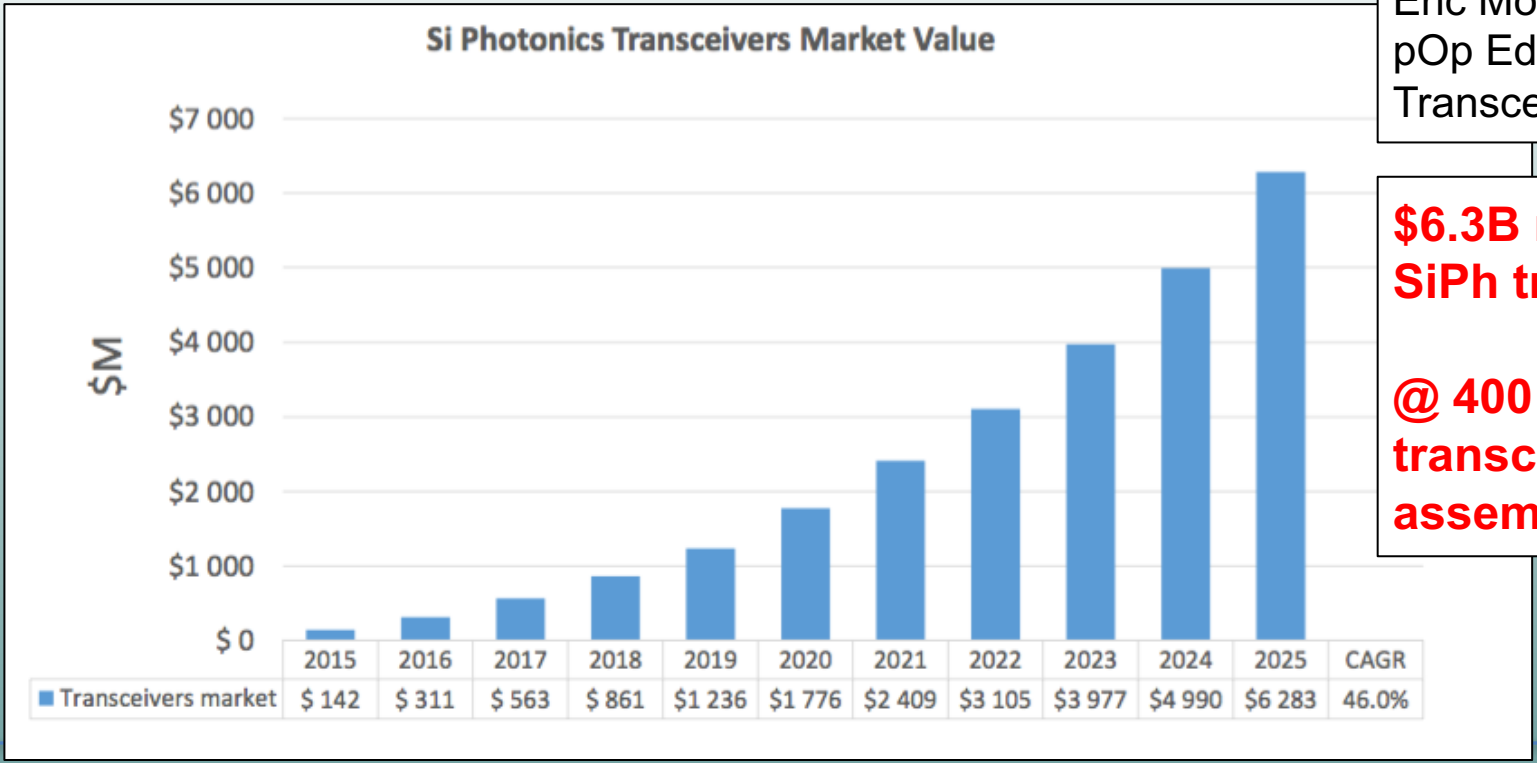
- Capital equipment cost (machine cost)
- Cost of ownership (flexibility, re-tooling, calibration, batch-changes, process – changes, recipes, etc.)
- **Cost per part**
  - Not a simple discussion ..
  - Assemblies / processes from few tens of seconds to several tens of minutes
  - Devices from few Euros to thousands of Euros
- **Assembly, TESTING, Packaging represents by far the highest costs of PICs**



'Process-Based Cost Modeling of Photonics Manufacture: The Cost Competitiveness of Monolithic Integration of a 1550-nm DFB Laser and an Electroabsorptive Modulator on an InP Platform', *Journal of Lightwave Tech, Vol. 24, No. 8, 2006. (from Peter O'Brien presentation at pOp, Edinburgh Nov 2016)*

Numbers and volumes (… and time to assemble and **test**)

- InP 2”-3” wafers and 12” SOI photonics wafers
- Are volumes increasing? Do we know the exact numbers?
- **There is more than telecom / datacom ….**
- **What does a machine manufacturer see? A steep increase of POs and multiple machines single orders**



	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	CAGR
Transceivers market	$ 142	$ 311	$ 563	$ 861	$1 236	$1 776	$2 409	$3 105	$3 977	$4 990	$6 283	46.0%

Eric Mounier, Yole,
pOp Edinburg Nov 2016,
Transceivers only !!

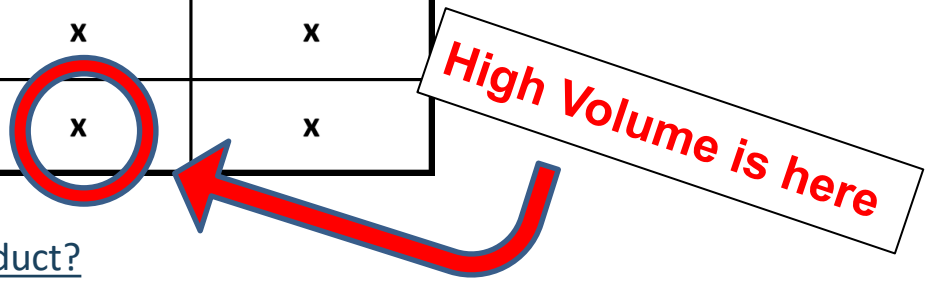
$6.3B market value for SiPh transceivers by 2025:

@ 400 USD for a 400 Gb transceivers > 15,75 M assemblies

Defining ‘Testing’….

Measurement: Characterization vs Testing

Technique	Scope: Verification	Scope: Validation
Characterization	x	x
Testing	x	x



SCOPE

Validation: Are we building the right product?
Design phase activity, to make sure that the design has addressed every requirement.

Verification: Are we building the product right?
Verify the functional behaviour. Prove that the design meets the requirements set out for it.

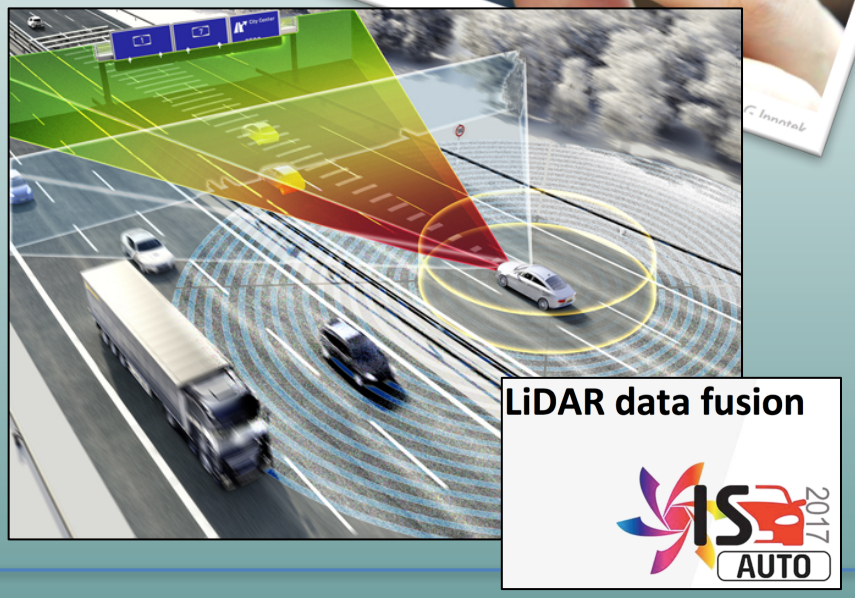
TECHNIQUE

Characterization: complex, refined, accurate and reliable. Parameters extraction, BB analyses, estimation of geometrical, physical and functional parameters. Requires skilled operators.

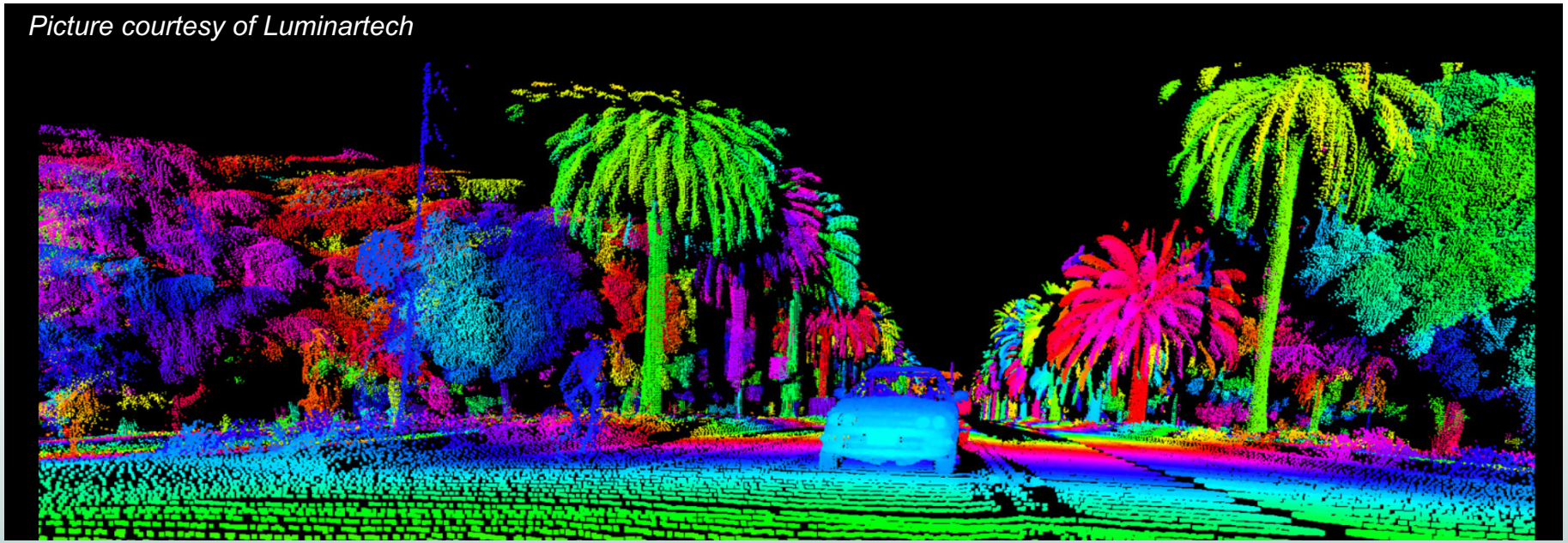
Testing: finding out how well something works. Routine probing focused on functional aspects. Repetitive, less sophisticated, wafer or bar level, (semi) automatic. Go-no go, statistics acquisition.

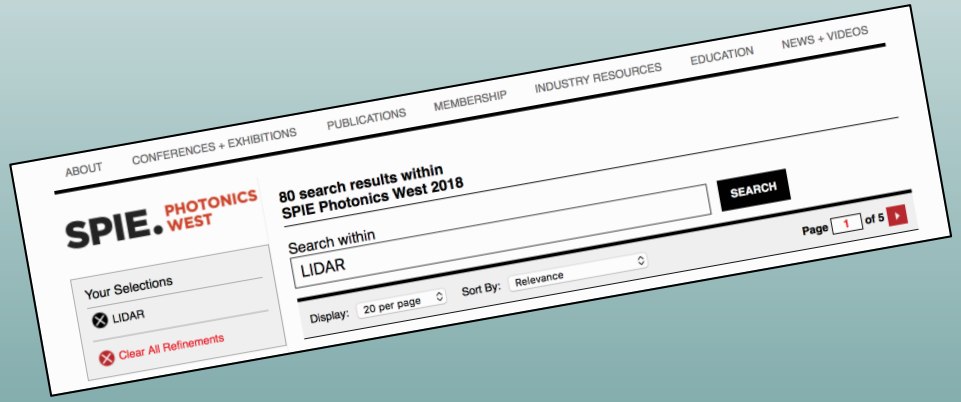
There is more than Telecom / Datacom ….

- Grateful that Data Centers & Cloud Computing have recovered photonics from the FTTH bubble of the late 90'ies / early 2000..
- Where is the future of Photonics?
- Biomedical (diagnostic at individual level ..)
- Sensing (everything that can be squeezed from an optical bench onto a chip)
- RF Photonics (aerospace, defence, …)
- Autonomous vehicles (cameras, LIDAR, …)
- IoT & Consumer goods
- …..



At PW 2018: LIDARs, AR-VR-MR, …





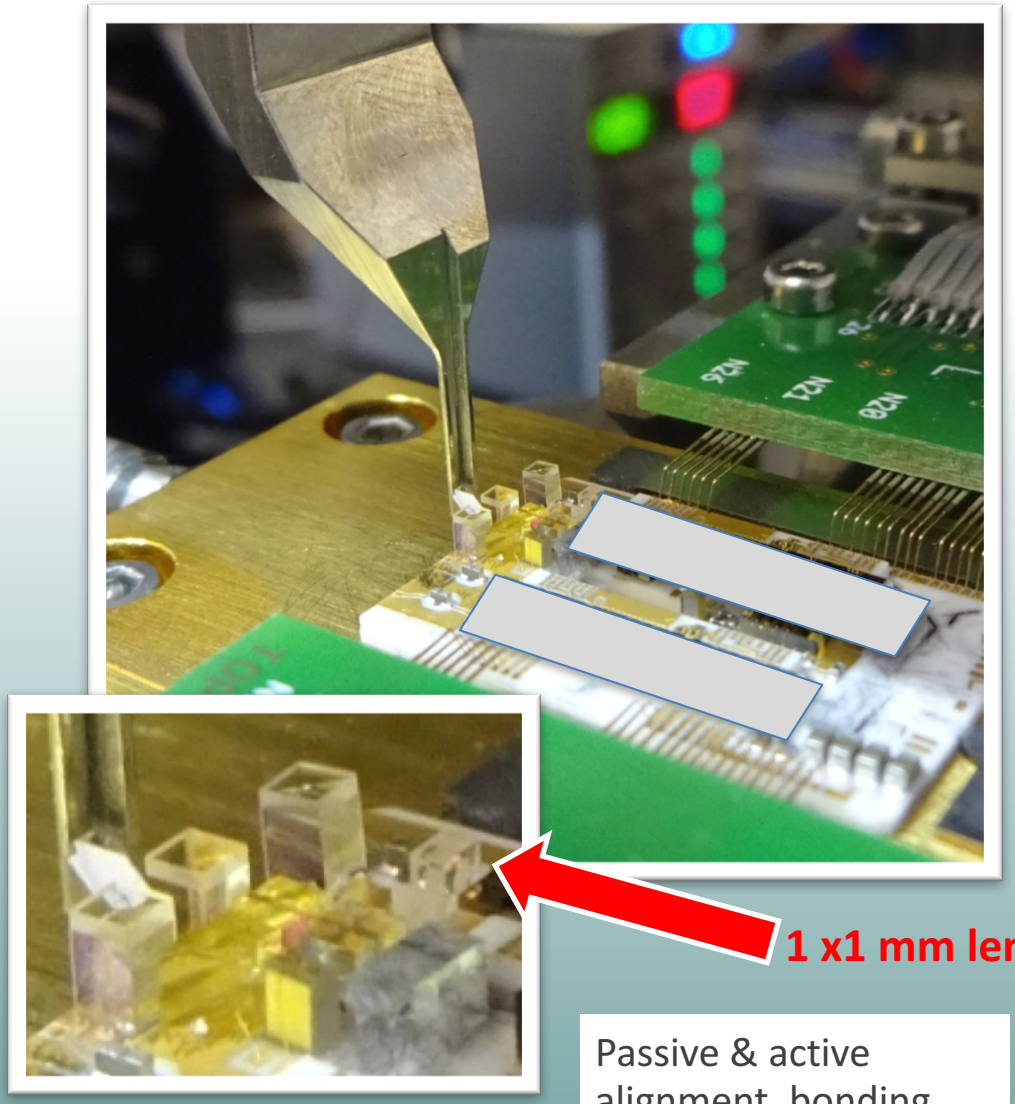
- 80 hits on SPIE program search ..
- Today LiDAR is ever present thanks to Autonomous Vehicles
- Testing Laser sources, PICs, sophisticated photodetectors, micro optics assembly ….

Testing in the assembly cycle

- In order to assemble you need to switch on your device and test ’something’ ….

Testing while you assemble, 1

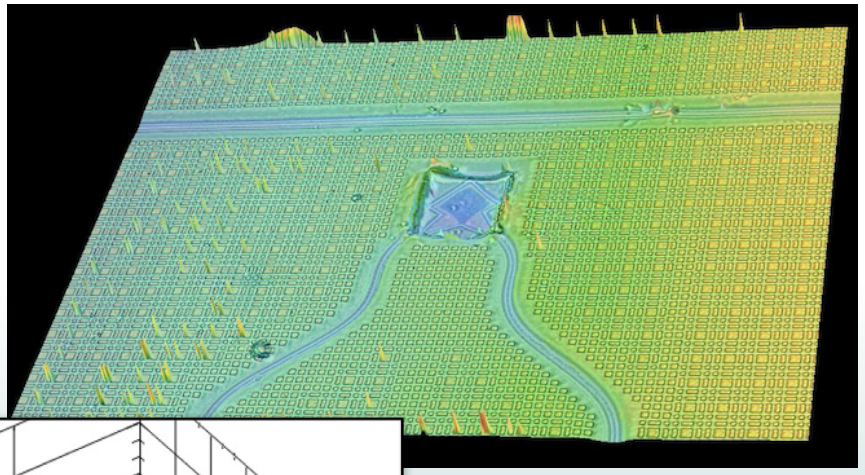
- Automated assembly starts with pick & place and requires passive & active alignment with sub-micron accuracy, bonding, testing, …
- **From 'simple' TOSA-ROSA (Transmitter / Receiver Sub Assembly) assembly to very complex applications with active/passive alignment of > 30 elements for complex fully integrated transceivers**
- **Testing (in-line)** is part of the assembly process **as reworking is almost impossible in most applications**

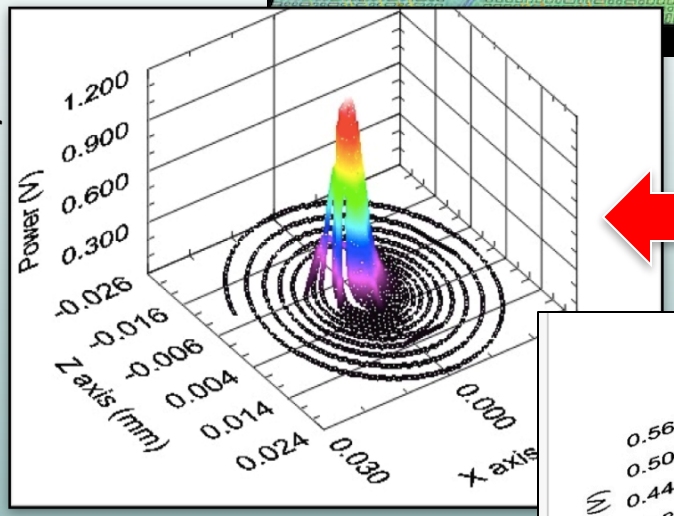


Passive & active alignment, bonding, electrical probing,

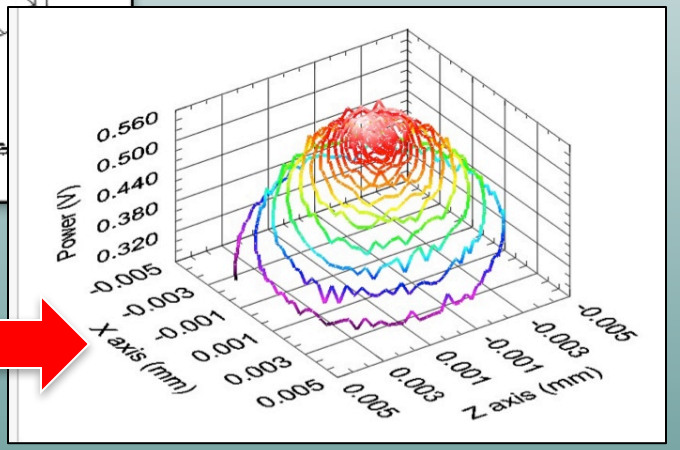
Testing while you assemble, 2

- **Active alignment is testing …**
- The sequence:
  - Passive alignment: locate coupling structure using machine vision geometric features detection and ensure ‘first light’
  - Fast active alignment: dither / spiral search over a reduce area / volume
  - Instrumentation: laser source + power meter ..
- Works well with both gratings and edge coupling with single or arrayed fibers





50 x 50 µm search area

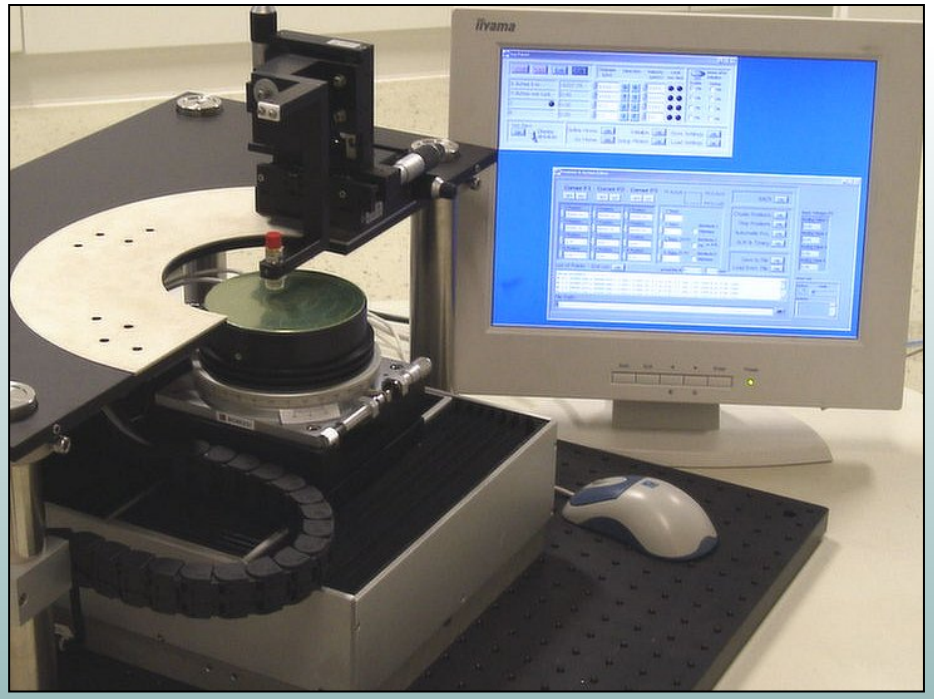


10 x 10 µm search area

Some examples of past work, 1

A 2“ wafer VCSEL tester from 2002

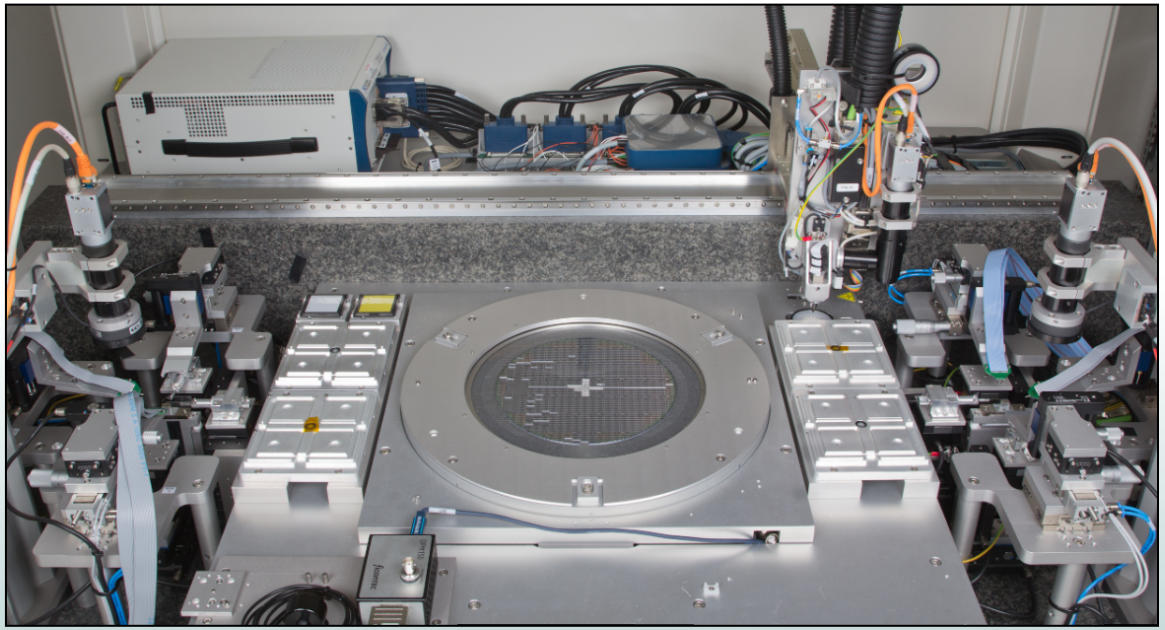
- Electrical and optical probing
- Tests 24/7 with 1s cycletime
- **Challenges today:**
  - on a 3“ wafer today you can have up to 50,000 VCSEL
  - **Approx 14 h per wafer ???? !!!!!**
  - And what about burn in?
  - Devices on a pitch of 200 – 300 µm
  - Number of contacts ...
  - Purely electrical?
  - Power dissipation?

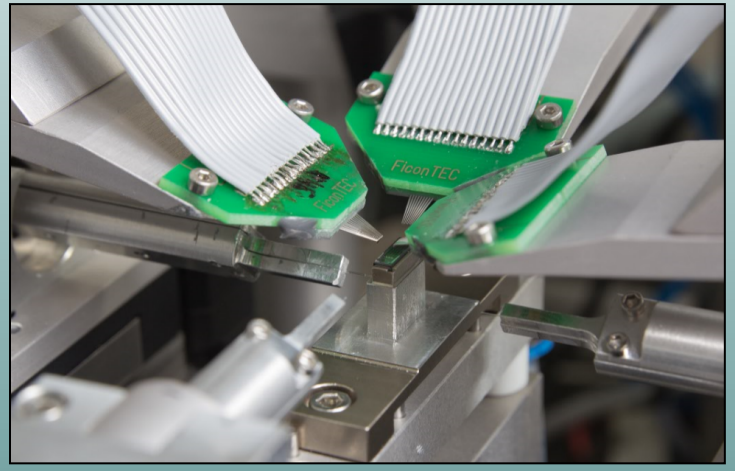


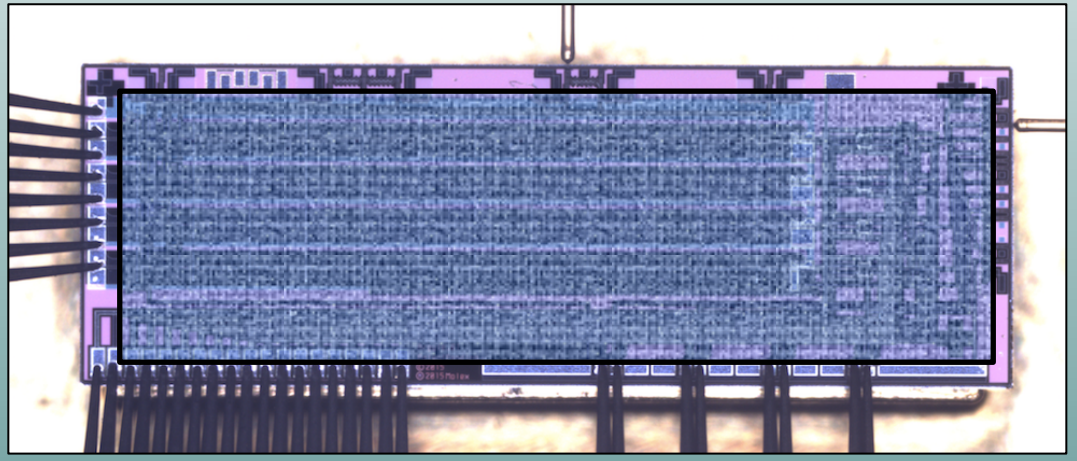
Some examples of (recent) past work, 2

Singulated SiP Chip edge-coupled tester

- 8“ or 12“ Wafer
- Pick, Place and Sorting
- 2 test stations
- 1s per optical channel (In-Out)test time
- Separated electrical & optical probing
- Fully integrated instrumentation & software



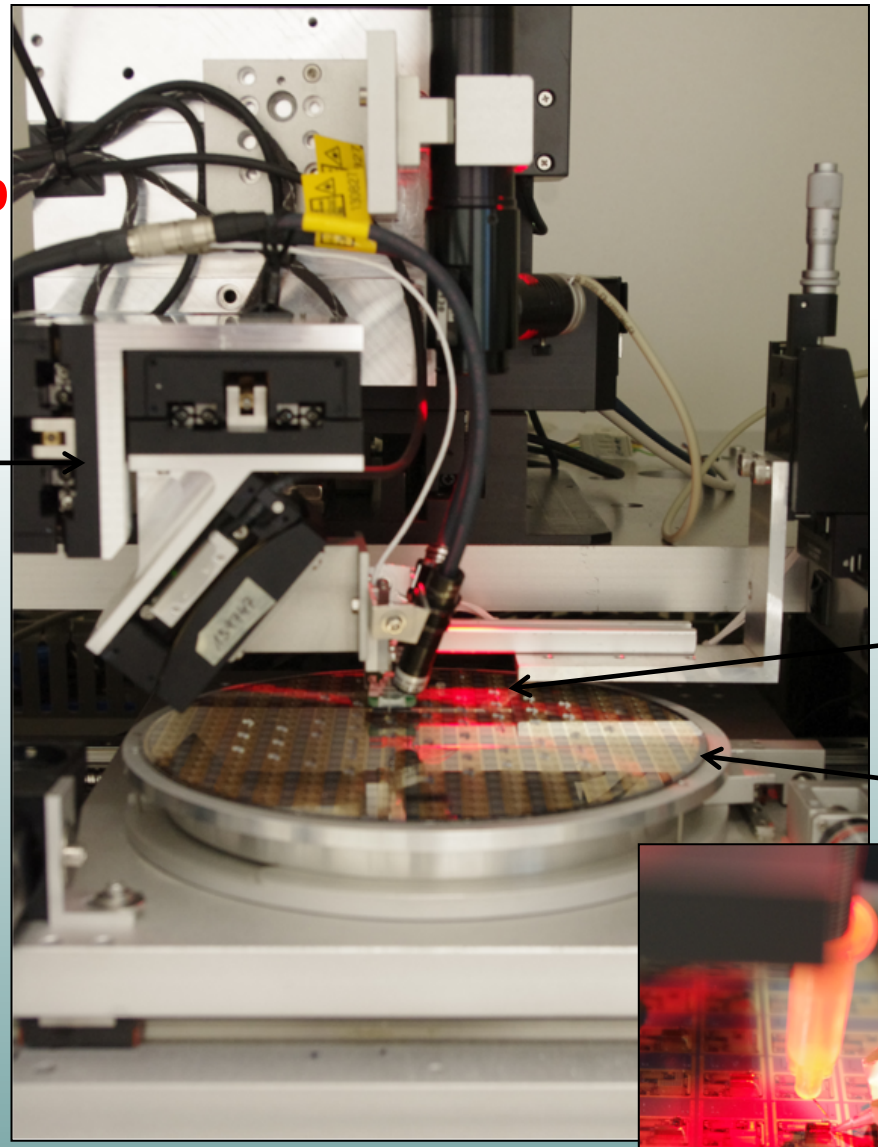


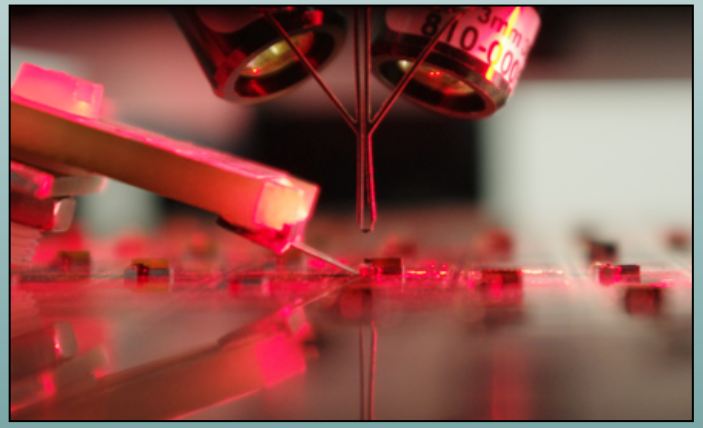


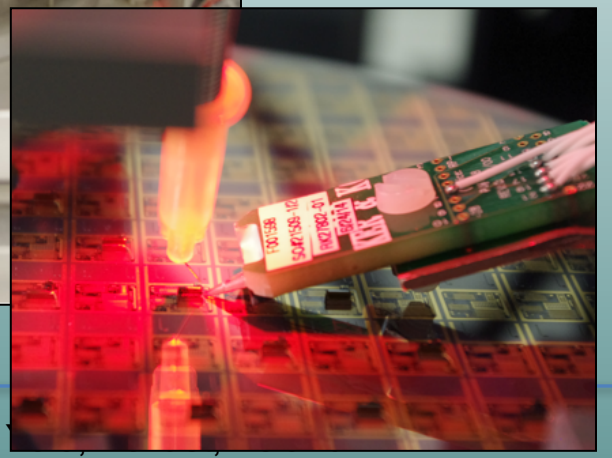
Some examples of past work, 3

ficonTEC assembly automation solutions

Early works on Wafer Level Test System SiP Chip







The wafer chuck & temperature management …

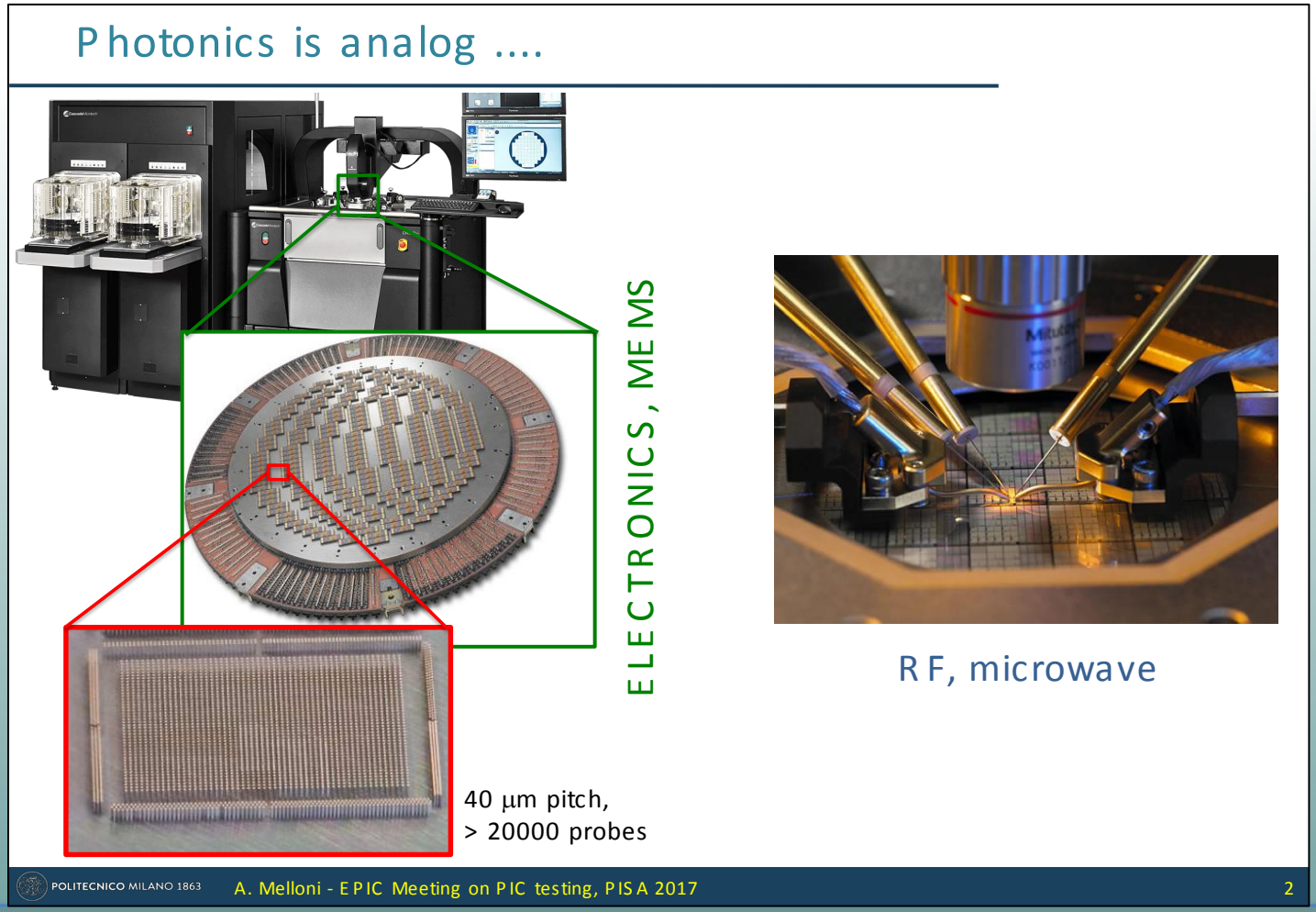
Temperature Range	+25°C to +200°C	
Extended Temperature Range	-30°C to +400°C	
Temperature Stability	±0,1°C	
Temperature Accuracy	±0,5°C	
Heating Rates	+25°C to +200°C	<10min
	-10°C to +25°C	<2min
Cooling Rates	+25°C to -10°C	<7min
	+200°C to +25°C	<8min
Chuck Diameter	205mm	
Temperature Uniformity	-30°C to +100°C	< ± 0,5K
	+100°C to +400°C	< ± 0,5%
Isolation	>2TOHM	at 25°C
Capacitance	1000pF	Standard
	100pF	triaxial connected
Chuck Dimensions	Diameter	205mm
	Height	28mm
	Weight	2750g

Moving to full wafer level & high volume testing

- Work in progress ….
- More work needs to be done
- The market does not yet have suitable products

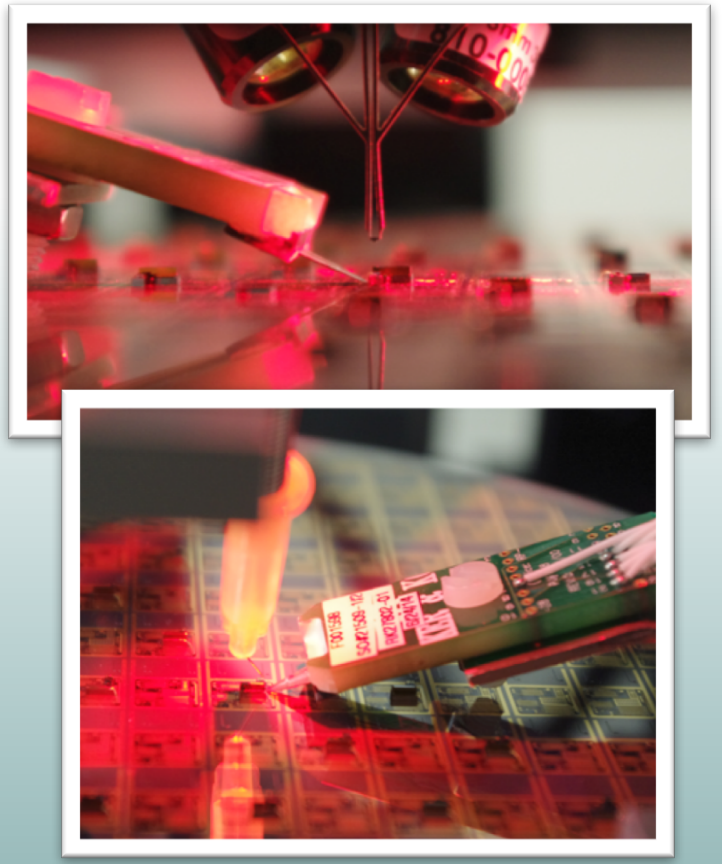
Photonics (PICs) vs semicon testing ..

- Very different pint counts ..
- Different parallelism paradigm..
- It is not sufficient to stick a couple of optical probes on existing equipment ….



Testing for volume production

- I would like to differentiate between full device characterization at an early stage, possibly with the first MPW project / first wafer runs
- And full volume testing either prior or during assembly
- The latter requires fastest possible testing, multi-channel low cost modular instrumentation, smaller footprint / reduced floor space in the clean room
- **High-volume wafer-level testing comes in on its own with the need of dedicated high-throughput equipment (and is closely followed by wafer-level assembly)**



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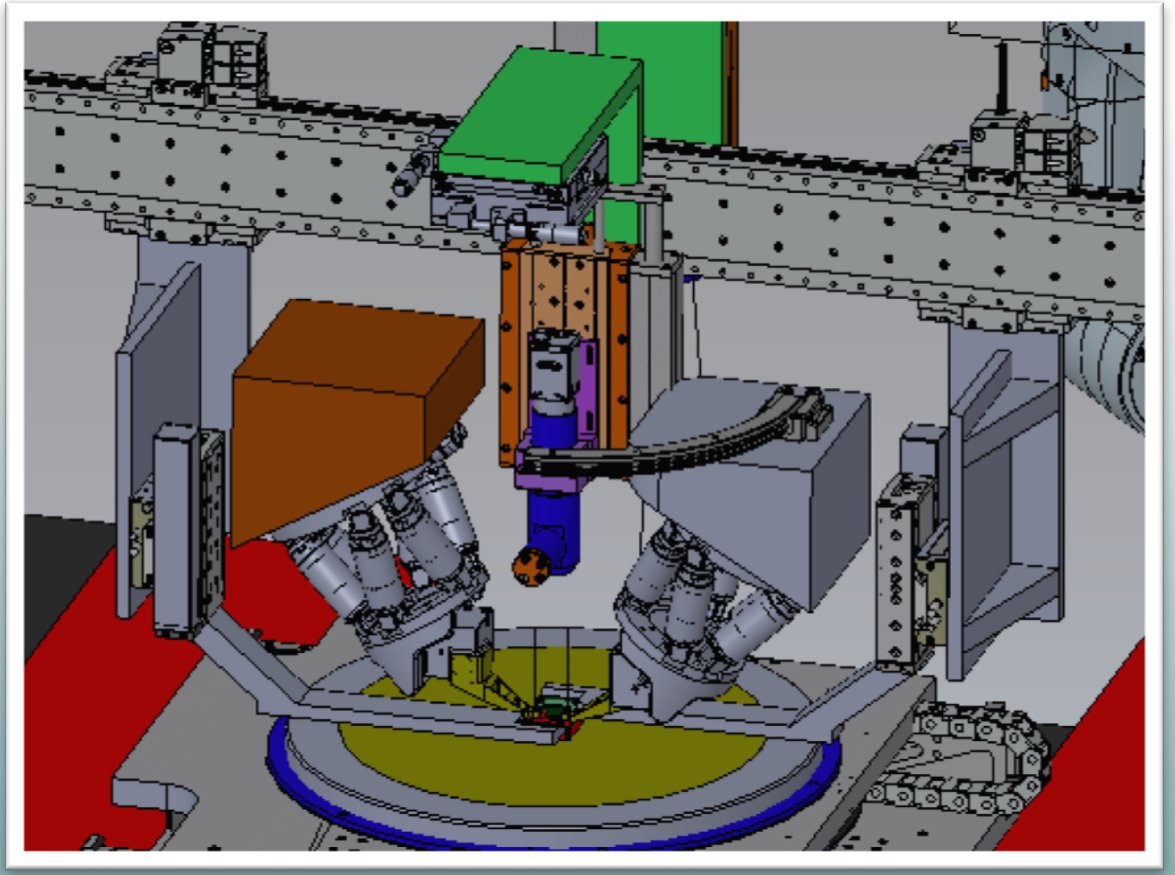
assembly automation solutions

Some on-going projects …

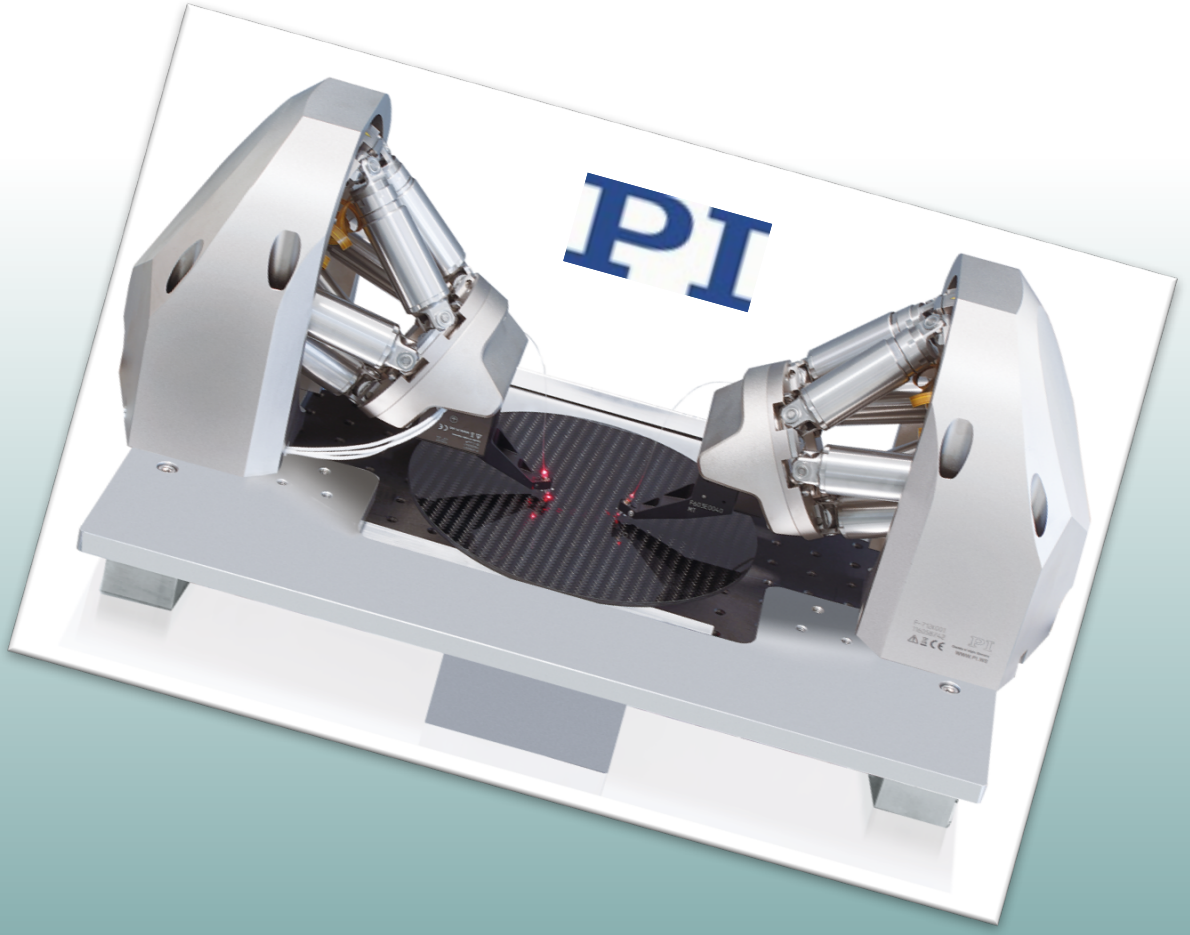
MPW / single chip-type full wafer-level testing

- There are strong needs / requests to perform wafer-level testing before dicing (top grating couplers & edge coupling)
- Combining electrical and optical testing is complex ..
- Testing comes before, during, and after assembly
- There is also a visible trend to perform assembly of hybrid components at WAFER-LEVEL
- In 2017 ficonTEC has been been awarded a PO for a new wafer-level tester complete with robotised wafer loading (AIM Photonics, USA)

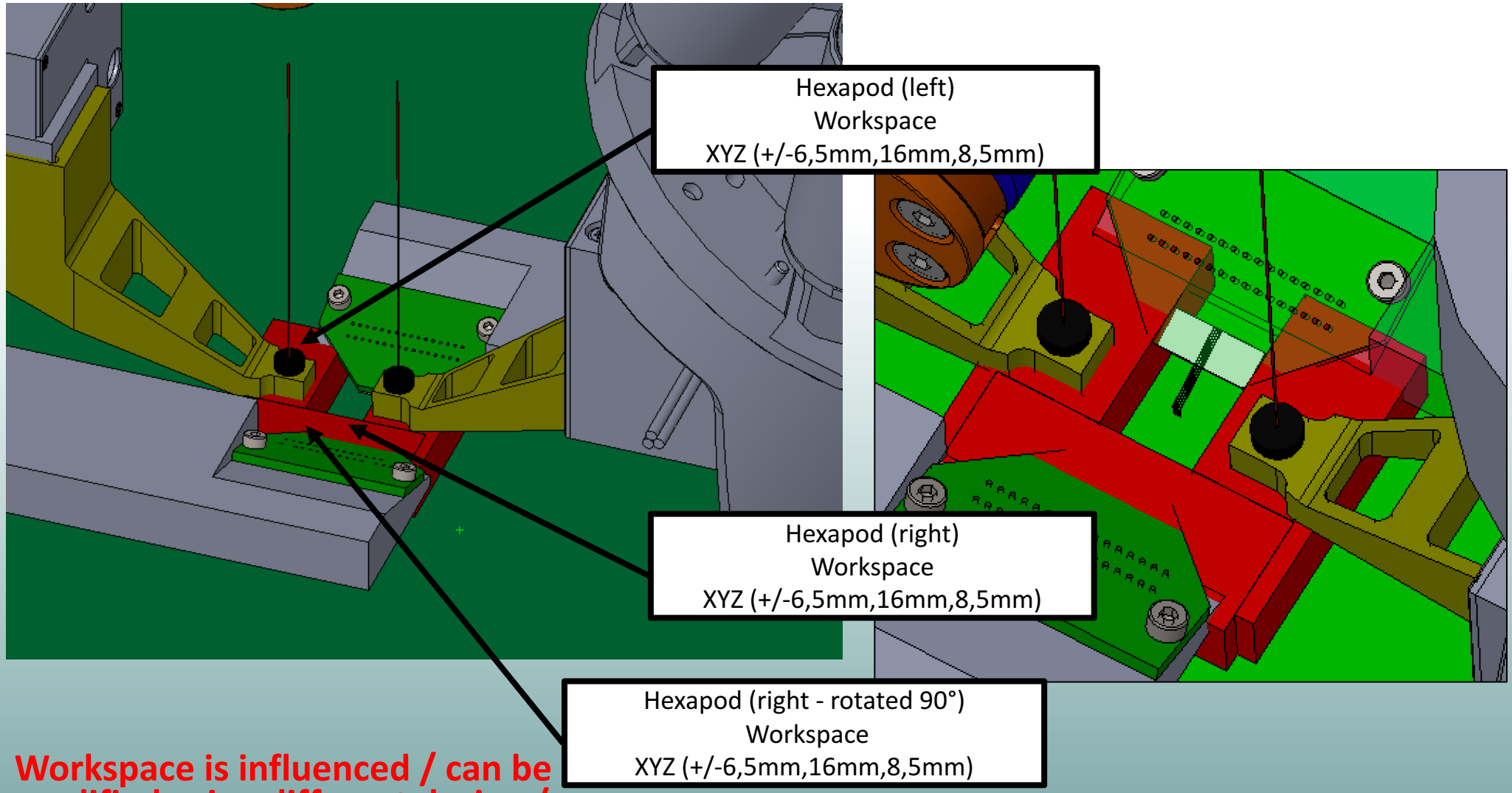


Accuracy and speed for optical alignment ..

- Adopting PI F12.HA2 platform
- But mounted upside down ..
- **And ADD all the other bits needed for a 'machine'**
- Multiple chip topology via combined wafer table translation & rotation



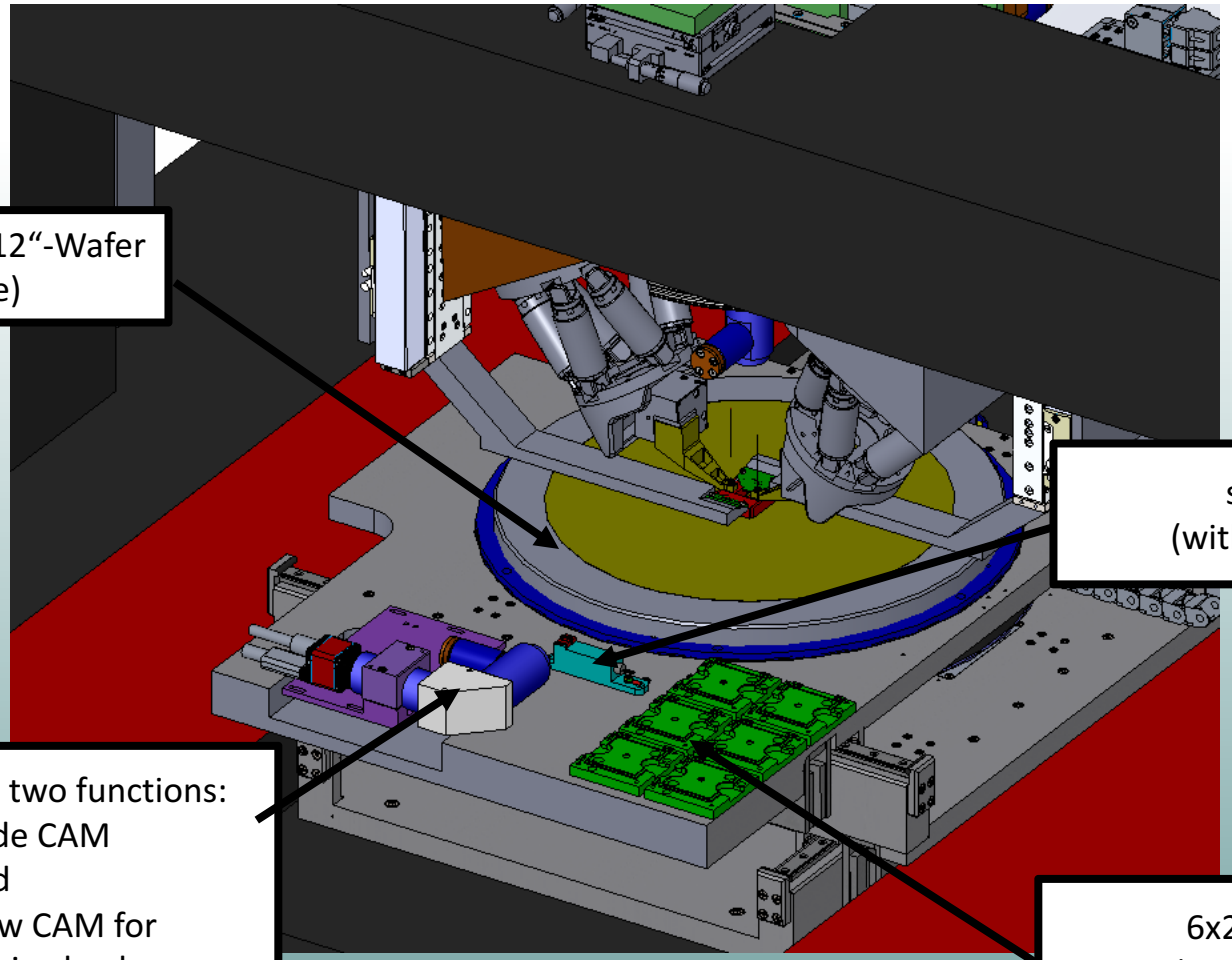
Hexapod workspace in 3D



Workspace is influenced / can be modified using different design / dimensions of probe holders

Wafer chuck area:

full wafers, singulated component on blue tape, Gel-Packs, …



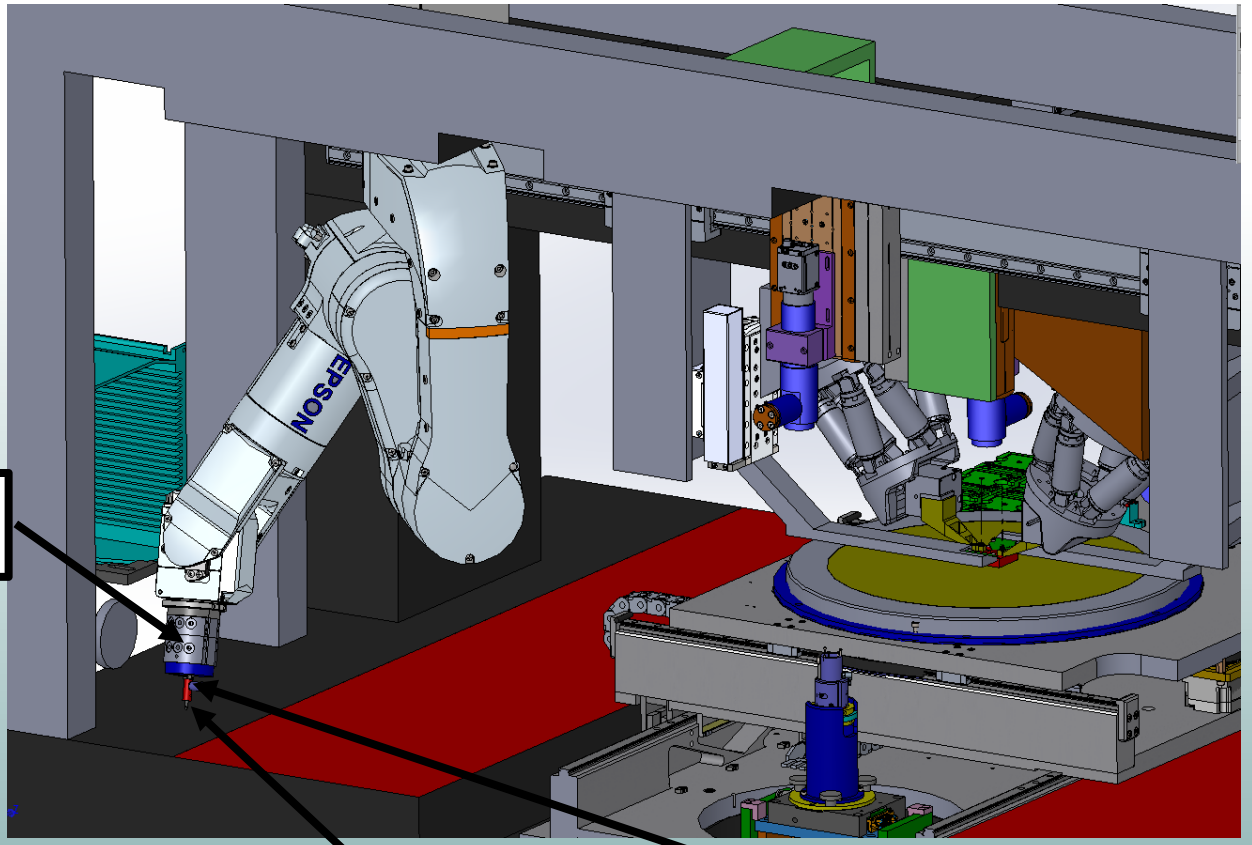
Wafer chuck for 12“-Wafer
(heatable)

single chip chuck
(with heating cartridge)

CAM system with two functions:
Bottom side CAM
and
front side view CAM for
the single chip chuck

6x2“ Tray for GelPak
(Vacuum release tray)

Rear view and Epson N2 robot



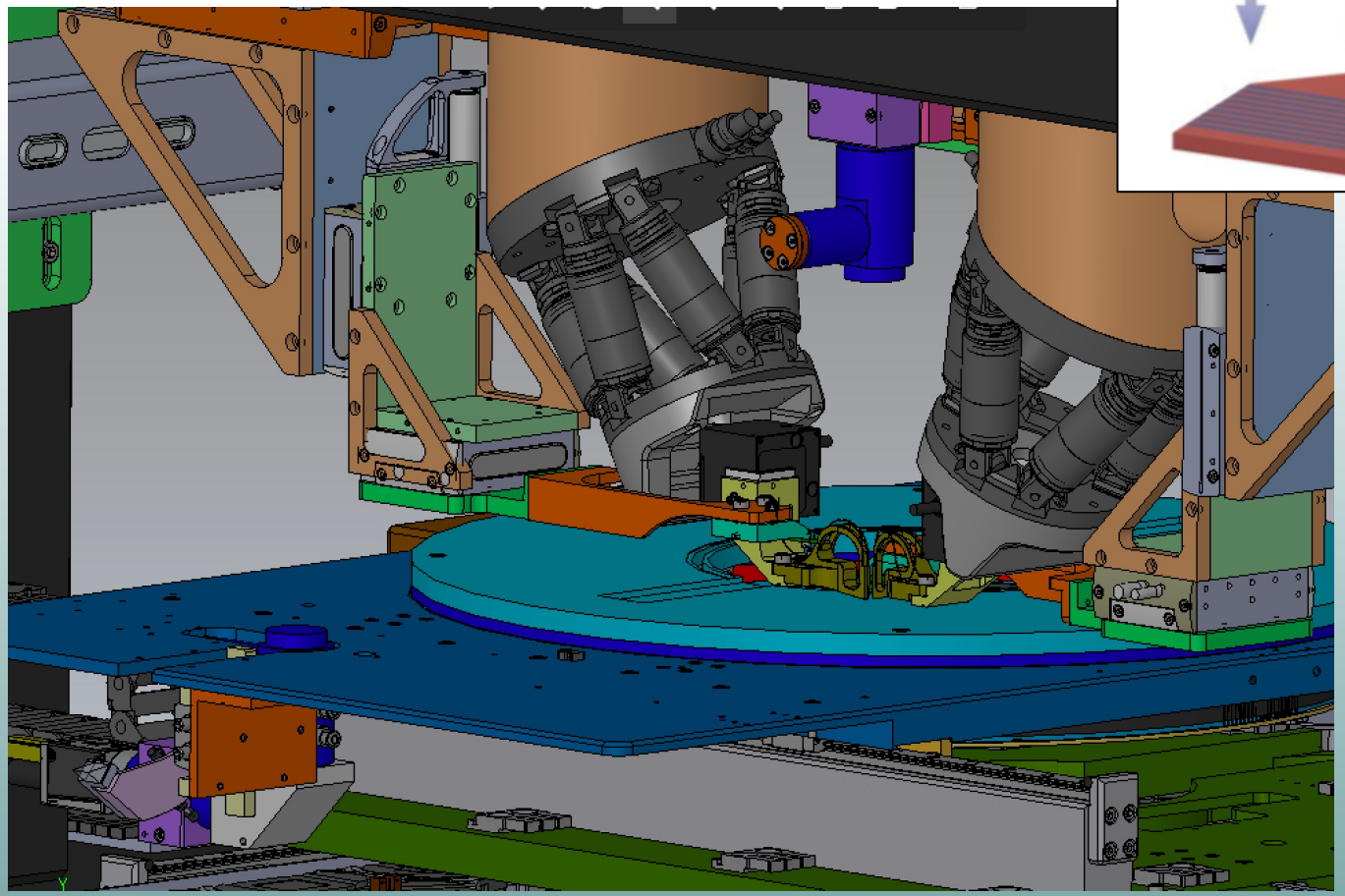
Tool interface

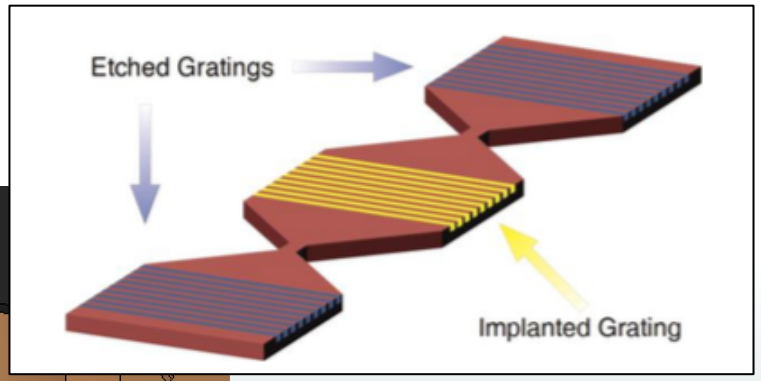
Force sensor
(only in Z-direction)

Pick up tool
For single chip

- **A general purpose 'handler' with automated flanged tools interface: wafer handler, singulated devices, …**
- **Clean room compatible**
- **Re- programmable for other auxiliary tasks: marking, auxiliary camera, …**

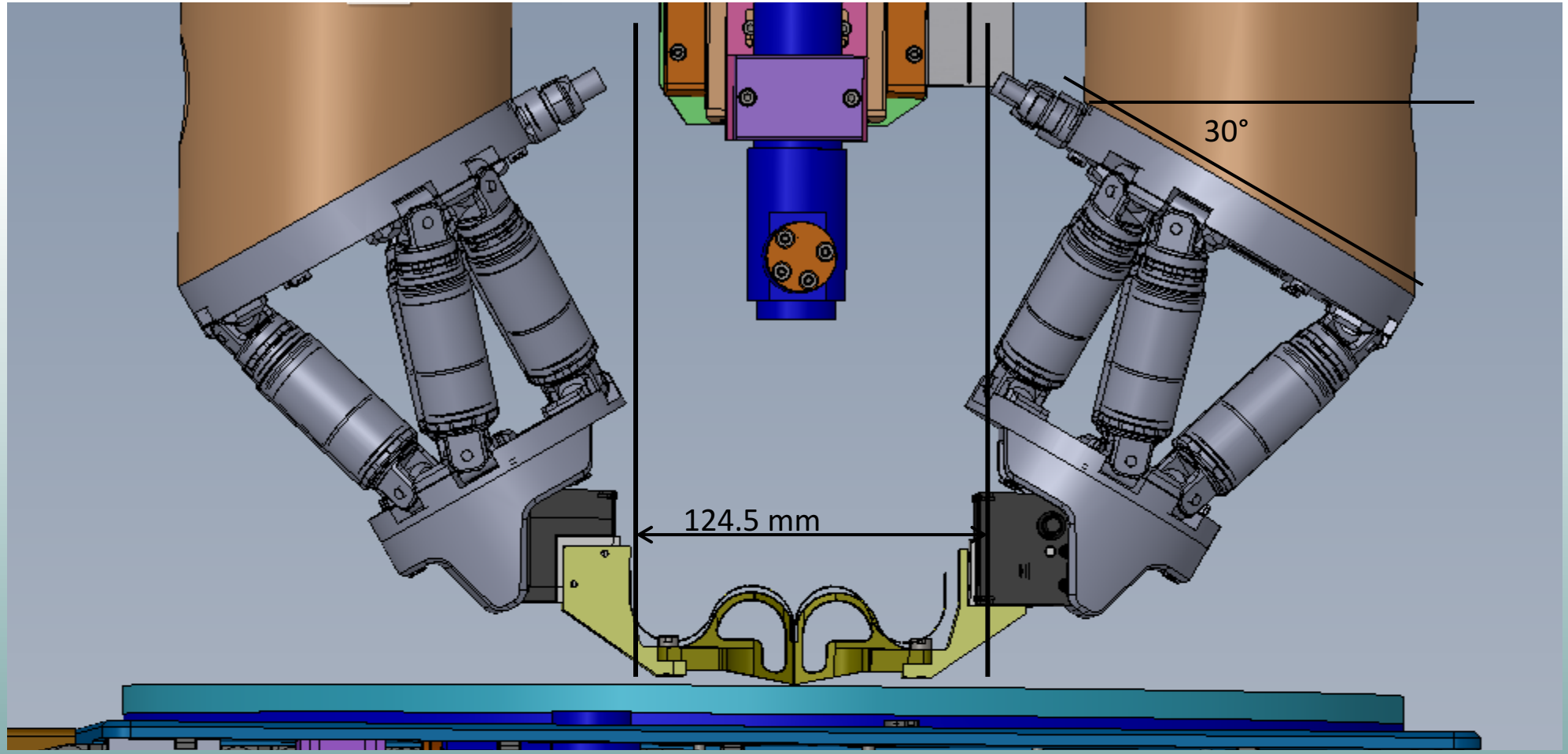
A specific project for SOTON University





- Erasable structures: SOTON
  - ‘removable optical test-point’ laser-ablated after use
- A machine for VALIDATION

Close spacing between fibers …

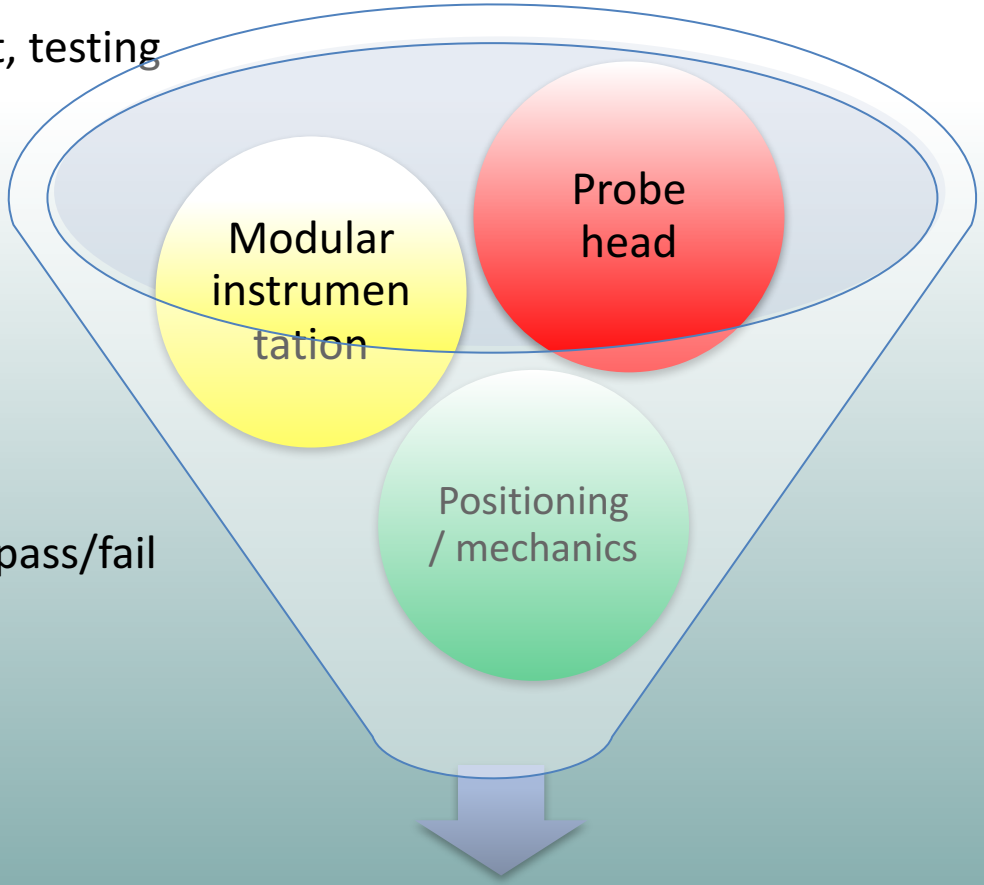


And some remaining challenges…

Three key areas being discussed / worked on

ficonTEC assembly automation solutions

- Hybrid probe head
  - Colours represent difficulty / priority levels
  - Requires some hard work, ideas, investment, testing
  - Technology from other companies
  - Combine optical / electrical
- Modular instrumentation
  - Adopt existing standards
  - Avoid rack & stack solutions
  - High end / low end
  - Differentiate between characterisation and pass/fail production testing
- Positioning /mechanics
  - We should have less problems of inyternal knowledge and skills
  - Speed, speed, speed

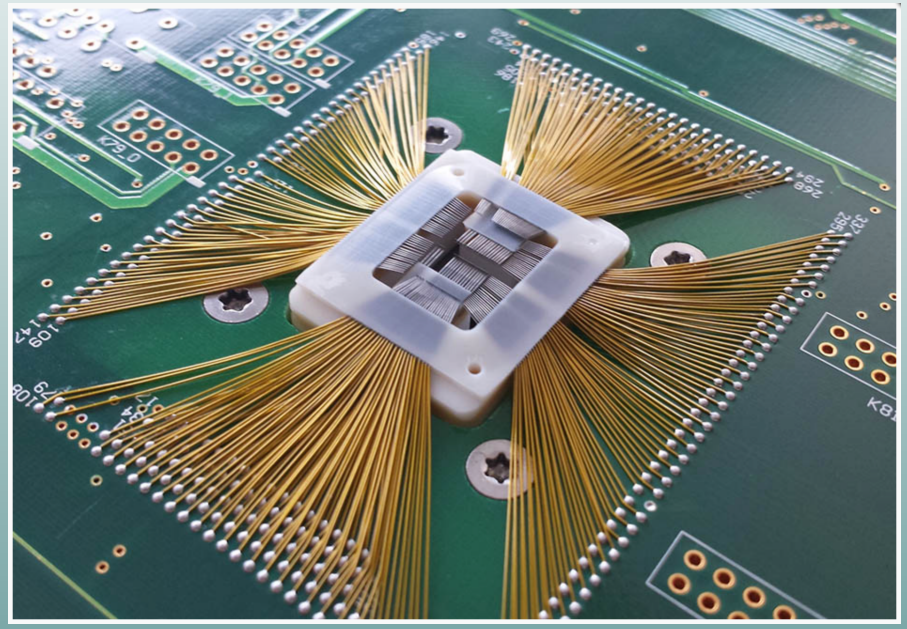


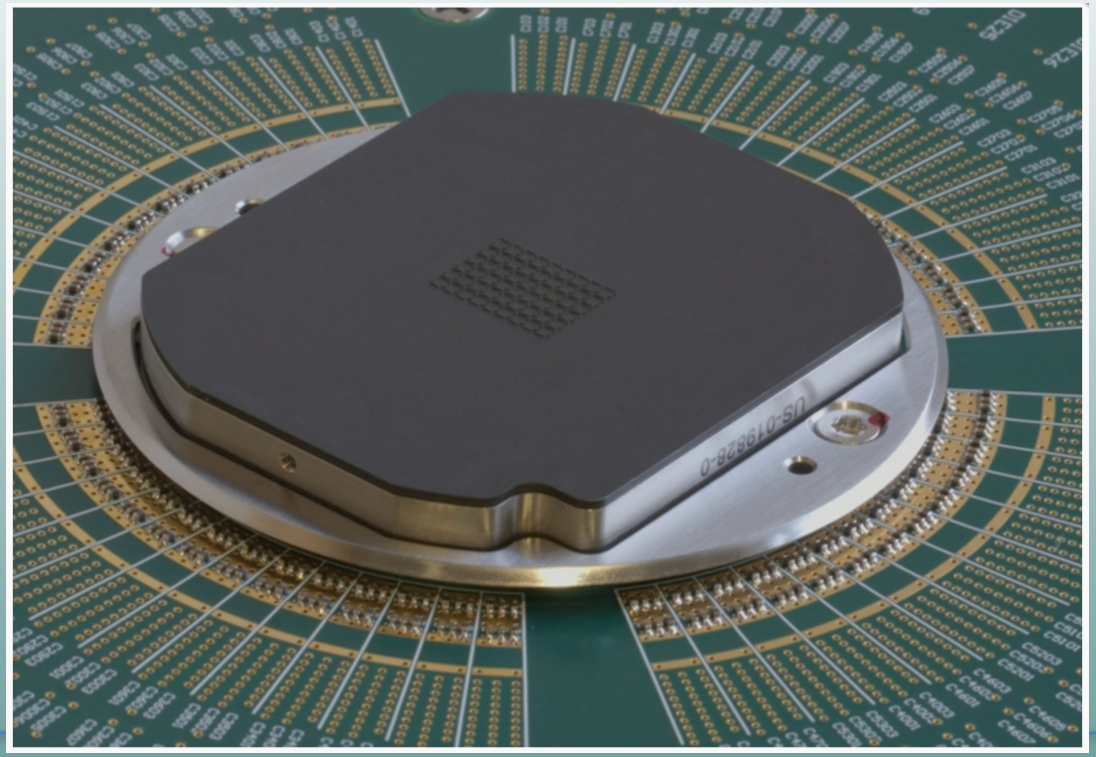
New family of machines …

‘Borrowing’ from semicon testing

- What is similar & what is different?
- Existing solutions on the market by a number of vendors could be integrated into the development of ‘combo’ probe heads:
  - Cantilevered probes
  - Micro-drilled ceramic plates
  - On-going discussions …….

Pictures courtesy of Technoprobe

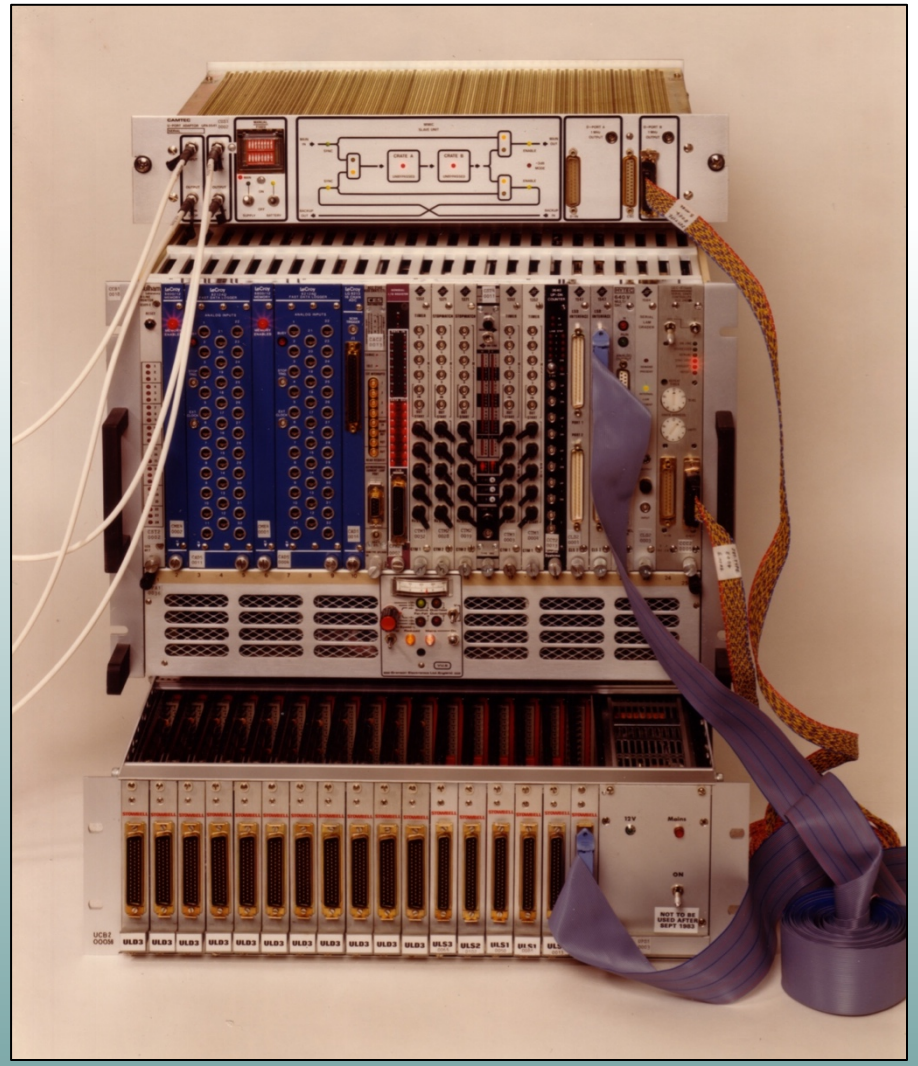




Some consideration for the probe heads

- In conventional semicon testing it is perfectly acceptable to purchase a specific probe-card – with thousands of pins - that can reach 100kEuro and massive electrical interconnect!!
- A hybrid probe head will not have the same pin count but still a PIC chip specific layout
- Input-Output spacing of optical probes must be accurate to 0.1 µm (vs a more relaxed positioning of electrical probes)
- We need to devise a method for pre-alignment of optical probing and some parallelism for wafer level testing

Modular instrumentation yesterday and today …



CAMAC: in my mid twenties on Nuclear Fusion research

Today on a PICs testing machine

Instrumentation: rack and stack vs modular / 1

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Adopt existing multivendor standards: PXI = PCI eXtended for Instrumentation

- One of this modules replaces 4 of these (not to scale) …
- **But not all instruments are available in modular form**

Instrumentation: rack and stack vs modular / 2

- Also adopt a non-multivendor lower cost platform (NI cRIO, FPGA based modular system)?
- Develop the missing PICs / optical test specific modules (both platforms?)

Optical / electrical measurements: what is really needed (an incomplete table …)?

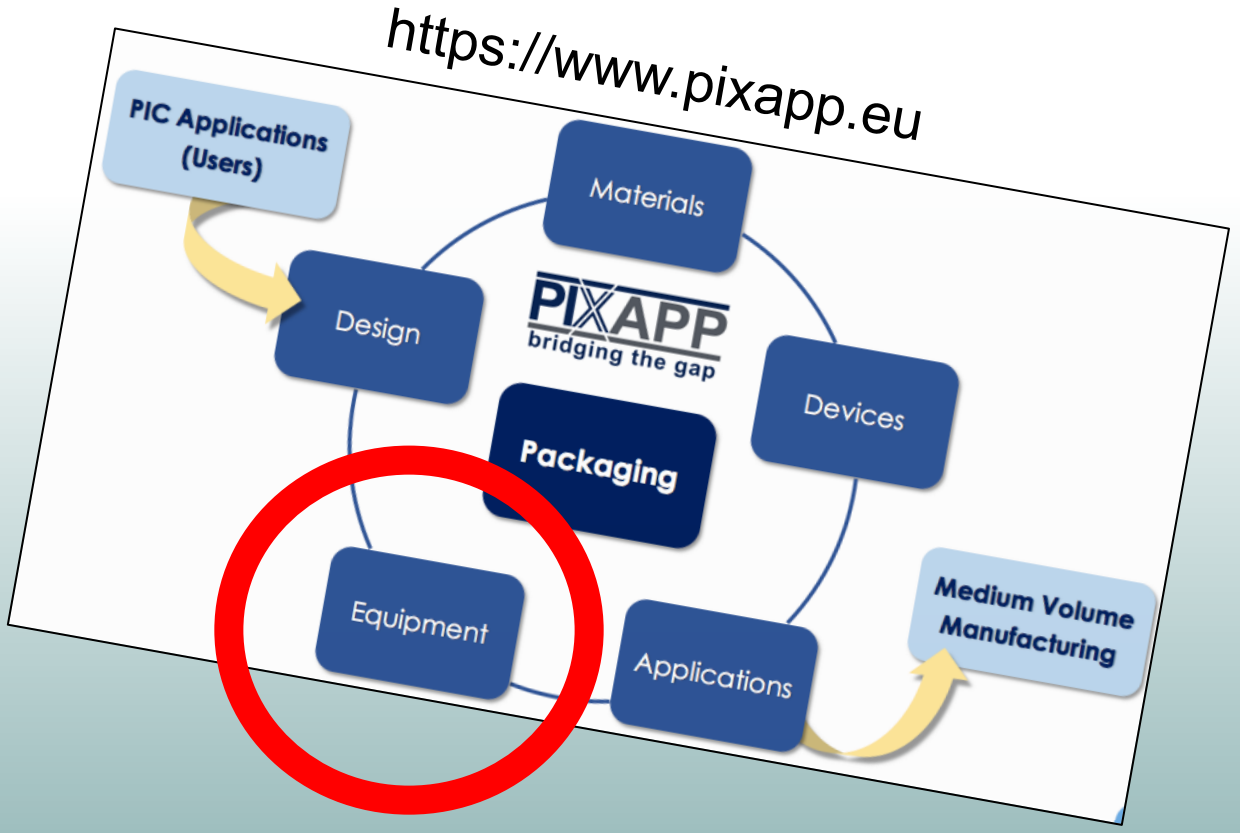
Optical	Electrical
Power level / insertion losses	DC / low freq Voltages / Currents
Polarisation?	
Modulation / bandwidth?	TIA / PD sensing
Light wavelenght?	Full RF measurements?
Optical sources	Temperature measurement and controls
Optical switching	……
……	……

Loading / unloading / contacting for burn-in …

- Before you test you need to pick & place, position, and carefully probe electrically and optically…..
- A message for our hosts **;-)** …..

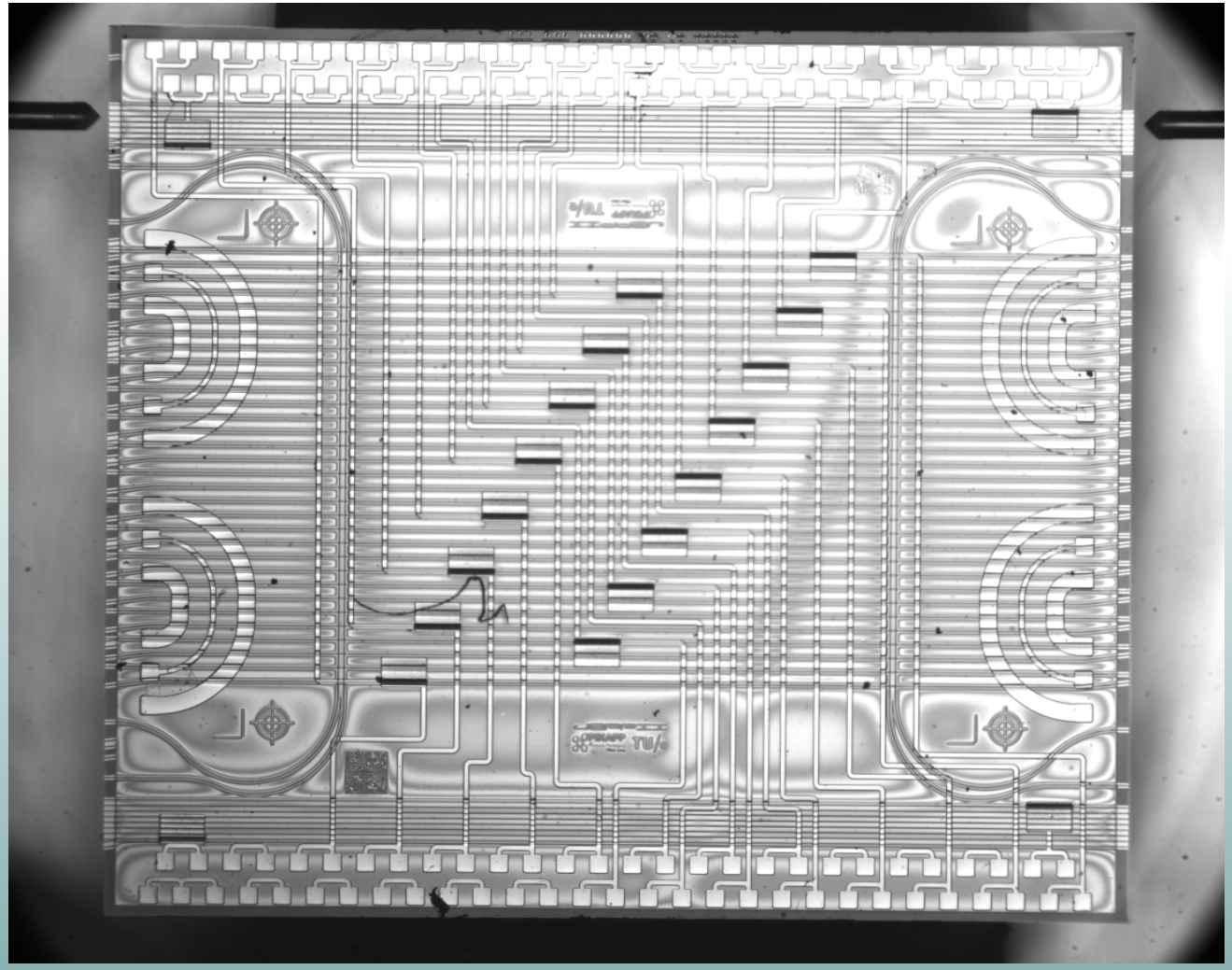
PIXAPP: a Photonics packaging Pilot Line in Europe

- What does a machine manufacturer get from this?
- A view of a complete PIC Packaging Supply Chain
- Linking design tools to automated assembly and test machines (design for test / design for automation)
- A 4-year interaction with very valuable partners
- A better understanding of PICs manufacturing & **TESTING** in different market segments
- **Extending outside PIXAPP ….**



PIXAPP
Photonic Packaging
Pilot Line

PIXAPP- TUe: getting access to test chips



View through top view camera
Edge coupled PIC with left / right optical I/O

A ‘playing’ station in our R&D ….

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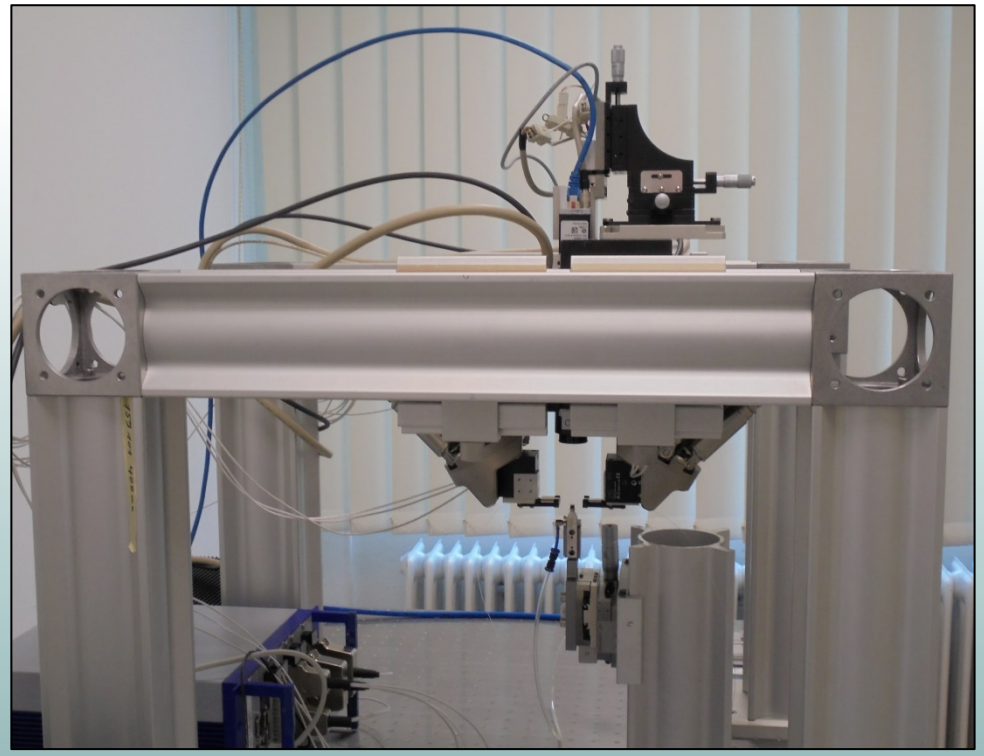
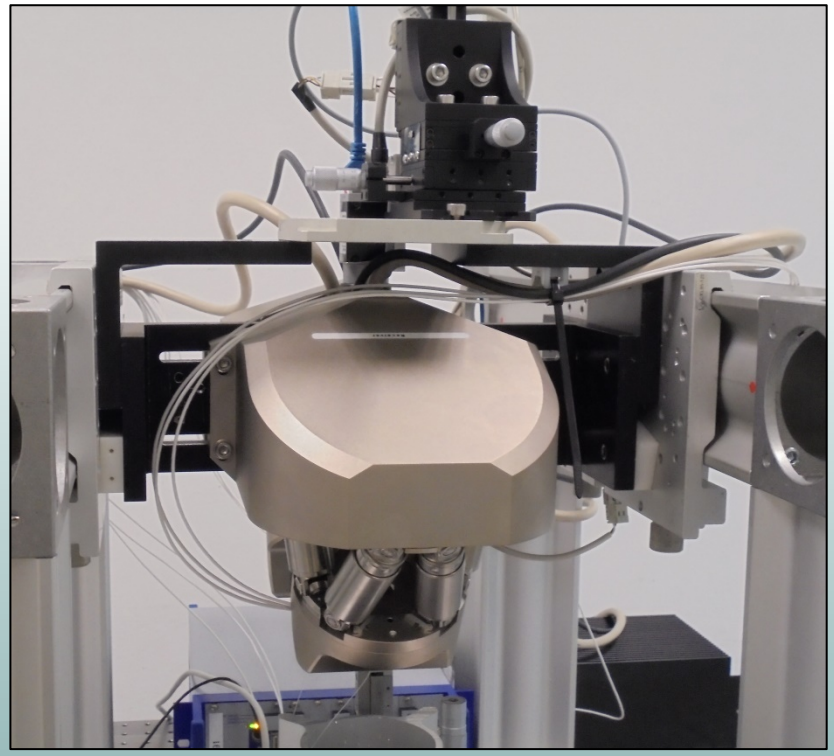


Side view



Back view

A very short video on in-out optical alignment

Conclusive remarks?

- As I said in Pisa I do not offer conclusive remarks …
- But I hope to stimulate some discussion and gather – with your help - a better understanding of the testing requirements for PICs ...
- **A collaborative approach with selected partners?**

THANK YOU
FOR YOUR ATTENTION !!
THANK YOU EPIC & YELO!!!

ANY QUESTIONS??

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